Profectis
Technischer Kundendienst

QUELLE.

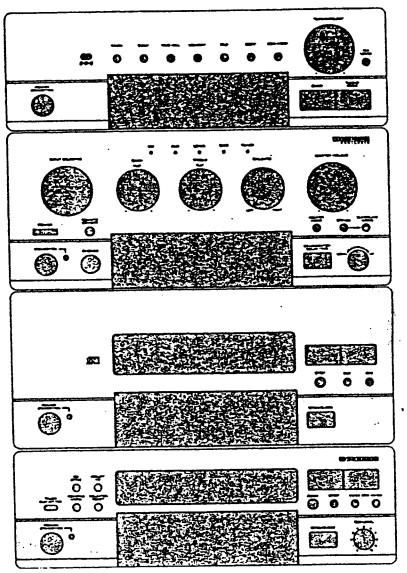
Serviceunterlage

(ET-Nr.: 216.238.6)

Produkt-Nr.:
035.751-7

Typ/Privileg-Nr.:
VTC-CD4096

Baustein-Set



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UTS-Nr.:          999         QUELLE
Best.Nr.:         0357517/01
Ger.Bez.:         UNIVERSUM-BAUSTEIN-SET

GKz:                G  GERAET
WGT:              653  STEREO-EINZELBAUST. ,BAUSTEINE-SET
KD-Sektor:          R  RUNDFUNK
BaumNr.:           00  KEIN DIAGNOSEBAUM VORHANDEN
Klassierung:      STG  STEREOG., TUNER, VERST., STEUERG
IFW-FehlerGru.:   205  RDF.,VERST.,TB.,PHONO,CD,CB
Type/Privileg/Universum.Nr VTC-CD4096
Beschreibung
VK-Preis: 1498.00

Serviceart:             01  PROFECTIS
Garantie fuer Kunden    12 Monate
Sondervereinbarungen:    0  SIEHE SERVICEART

Garantiereparatur       0004063  PROFECTIS GMBH
Sondervereinbarungen:          0  SIEHE SERVICEART

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Katalog                                          Seite
  Erst  994 HAUPTKATALOG H/W 99                   1409
  Letzt 000 NOCH IM AKTUELLEN KATALOG             0000

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Geraete Info:

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Technische Daten:

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Fehler:
  1 DIVERSE FEHLER
     DIVERSE FEHLER: SIEHE FEHLERBESCHREIBUNG DER
     ANLAGEN QBNR:036765 BZW. 038035
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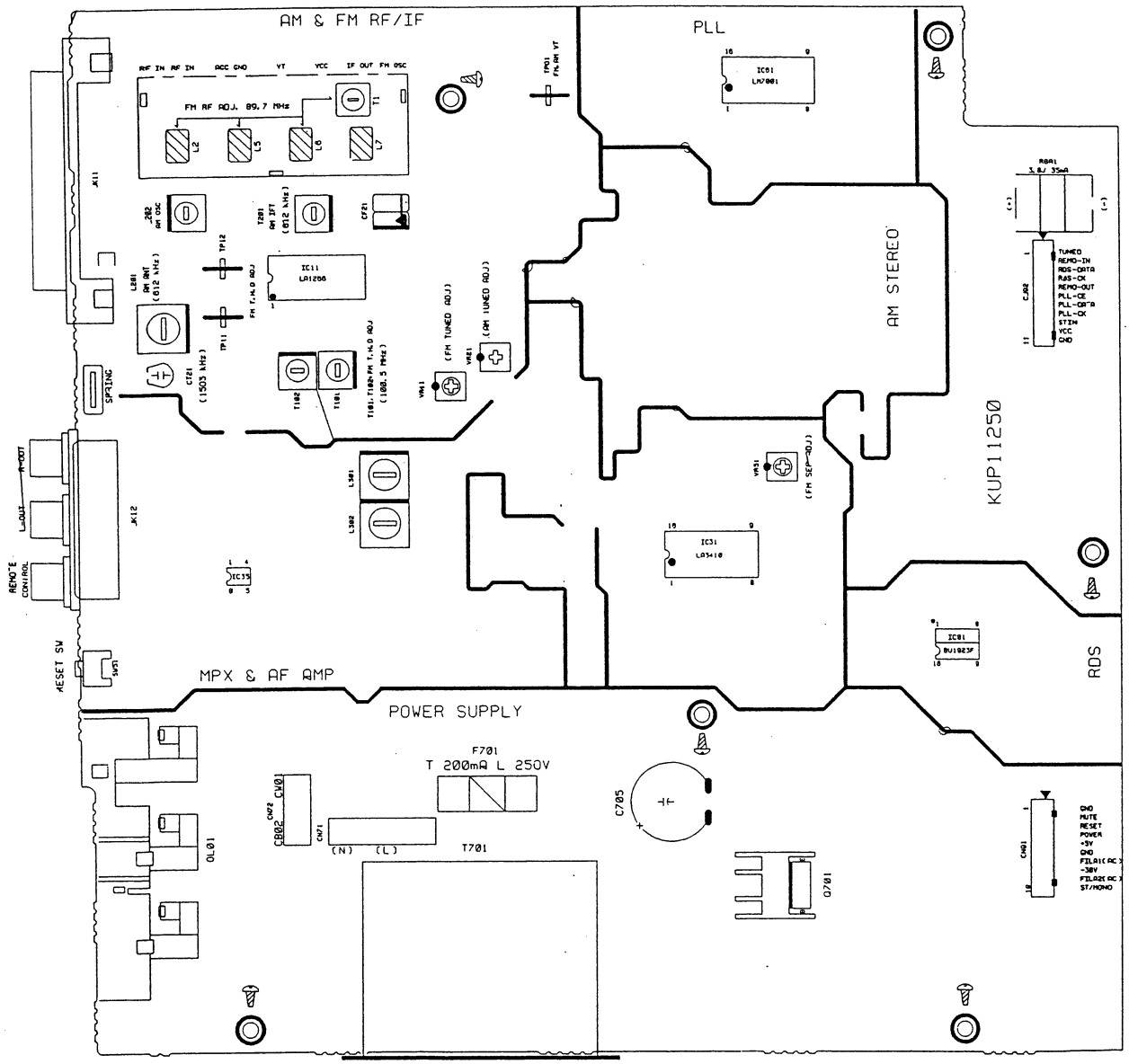
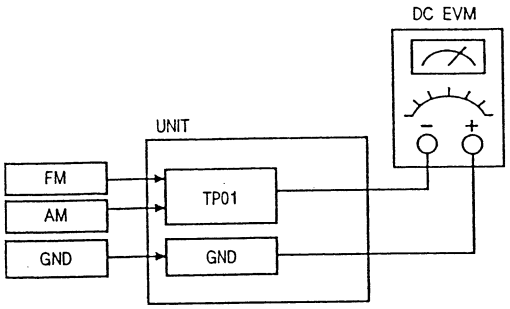
Nachdruck nicht gestattet
Änderungen vorbehalten


AM & FM RF/IF
PLL
AM STEREO
KUP11250
RDS
MPX & AF AMP
POWER SUPPLY
RESET SW
REMOTE CONTROL
FM RF ADJ. 89.7 MHz
IC11 LA1266
IC81 LA7001
IC31 LA3410
IC91 BU1923F
(FM TUNED ADJ)
(AM TUNED ADJ)
(FM SEP ADJ)
F701
T 200mA L 250V
T701
TUNED
REMO-IN
RDS-DATA
RDS-CK
REMO-OUT
PLL-CK
PLL-DATA
PLL-CE
+11V
GND
MUTE
RESET
+5VEX
+5V
GND
+8V
FILAC AC
-8V
FILAC AC
ST/MONO

MEASUREMENTS AND ADJUSTMENTS

1. TUNING FREQUENCY RANGE ADJUSTMENTS

(FM, AM) DC VOLTMETER ·····CONNECT TO TEST POINT TP01 and GND

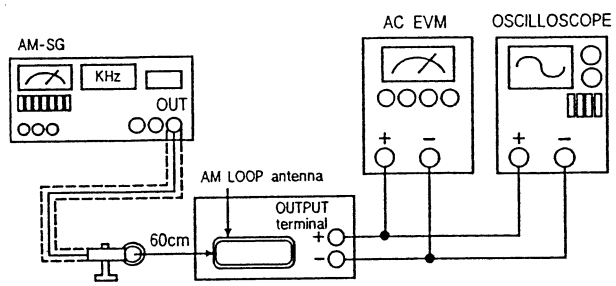


No	Band	Frequency	Adjust for	Adjustment
1	FM	87.50MHz	1.5V	L7
2	AM	522KHz	1V	L202

2. AM TRACKING ADJUSTMENT

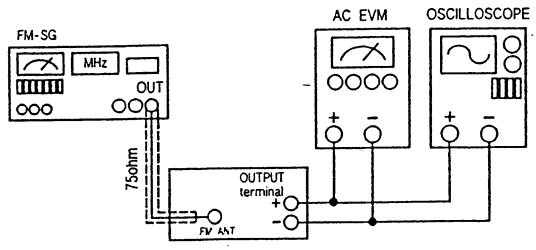
Signal Generator ·····Connects to the AM Ant. Coil through the loop antenna.
Adjust for the indication of VTVM of the wave form of scope to be maximum.

BAND	Step	Frequency	Adjust for	Adjustement
AM	1	612KHz	Maximum sensitivity	L201, T201
	2	1503KHz	Maximum sensitivity	CT21
	3	Repeat steps 1 and 2 several times		



3. FM-RF ADJUSTMENT

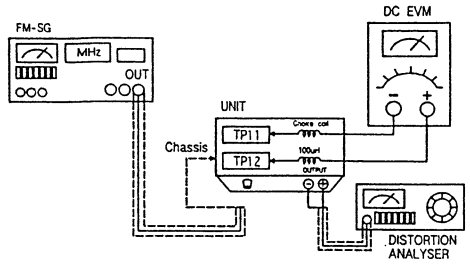
Signal Generator·····Connect to FM ANT JACK (FM IN) through the dummy.



No	Frequency	Adjust for	Adjustment
1	90.10MHz	Maximum Sensitivity	L2, L5, L6
2	Repeat step 1 several times		

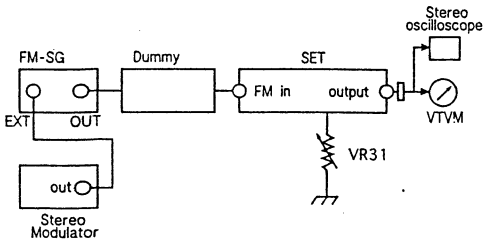
4. FM MONO DISTORTION ADJUSTMENT

DC VOLT METER ·····Connect to TP11(-), TP12(+) Through the choke coll (100μH)
Signal Generator ·····Connect to FM ANT Jack (FM IN) through the dummy.
Distortion Meter·····Connect to the output.



No	Frequency	Adjust for	Adjustment
1	100.10MHz	DC Voltmeter 0V	T101
2	100.10MHz	Minimum T. H. D	T102
3	Repeat steps 1 and 2 Several times.		

5. FM STEREO SEPARATION



Pilot signal	Adjust for	Adjustment
ON	Different of R and L must be maximum	VR31

NOTE : In case of adjusting the stereo separation, of input is L (or R) channel, R (or L) channel must be maximum.

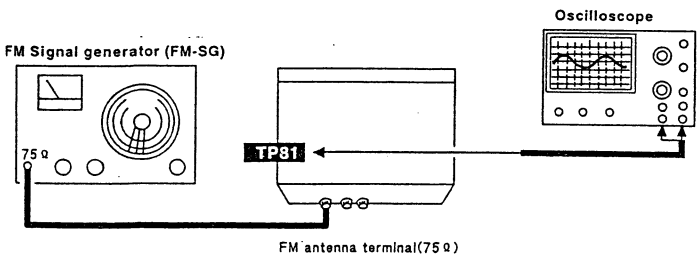
6. FM/AM AUTO STOP LEVEL ADJUSTMENT

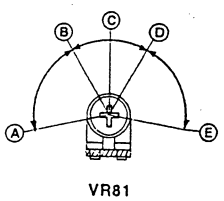
FM SIGNAL GENERATOR ·····Connec to FM ANT Jack(FM IN)through the dummy
AM SIGNAL GENERATOR·····Connect to AM ANT, Coil through the Loop antenna

BAND	STEP	SIGNAL GENERATOR	Adjust for	Adjustment
FM	1	100.1MHz 35dB	TUNED Display OFF	VR11
	2	100.1MHz 35dB	TUNED Display ON	VR11
AM	1	999KHz 80dB	TUNED Display OFF	VR21
	2	999KHz 80dB	TUNED Display ON	VR21

7. FM RDS ADJUSTMENT [EUR]

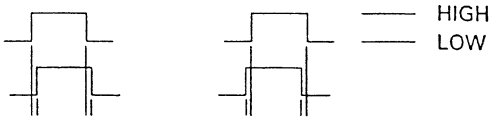
FM Signal Generator(RDS IN) ·····Connect to FM ANT Jack(FM IN) through the dummy
Oscilloscope ·····Connect to TP81(+) GND(-)

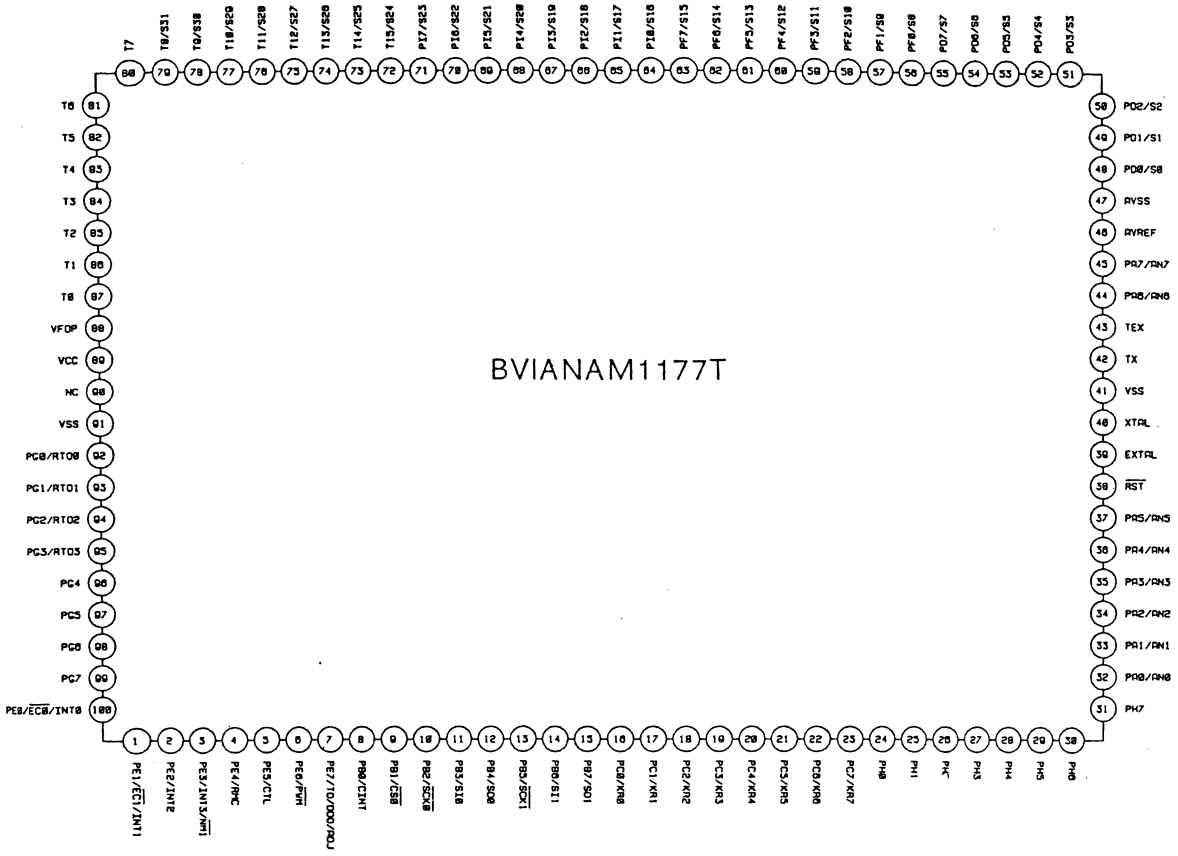


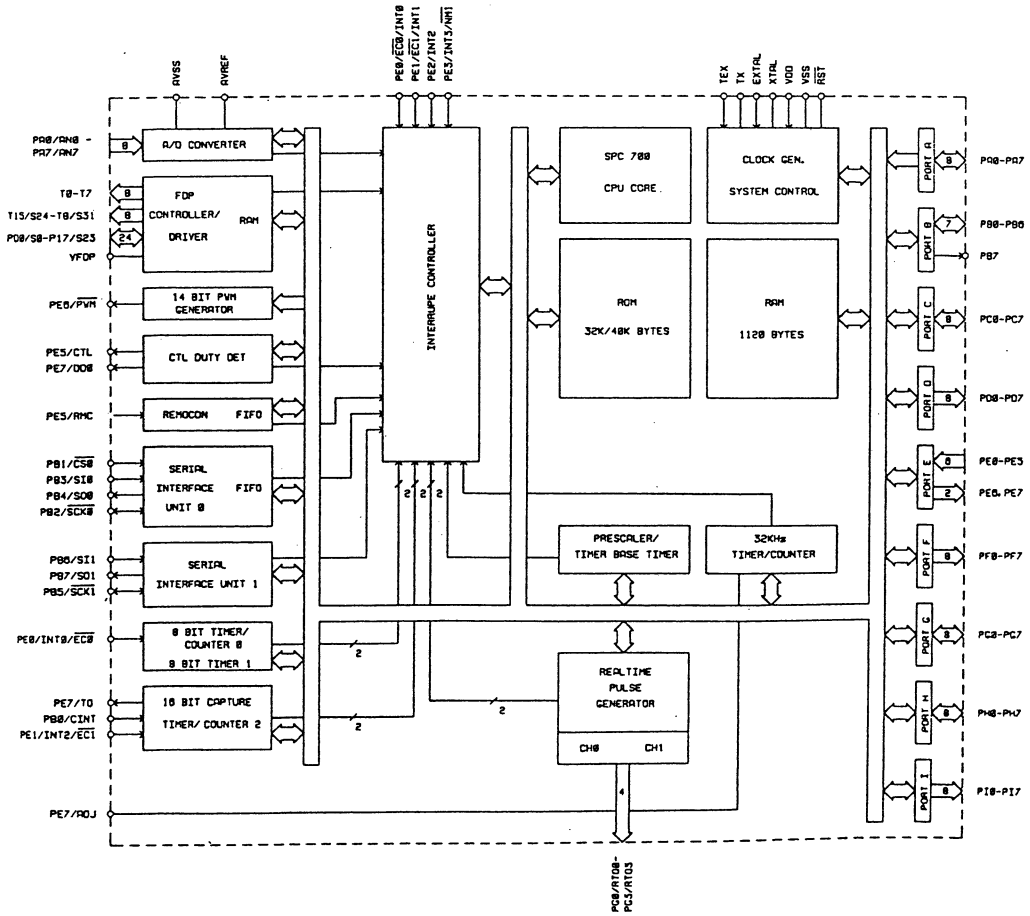


Ⓐ-Ⓑ, Ⓓ-Ⓔ : RDS OFF position.
Ⓑ-Ⓓ : RDS ON position. (indicator lighting)
Ⓒ : Adjust point of RDS circuit. (TP81 : 1.0~1.2V)

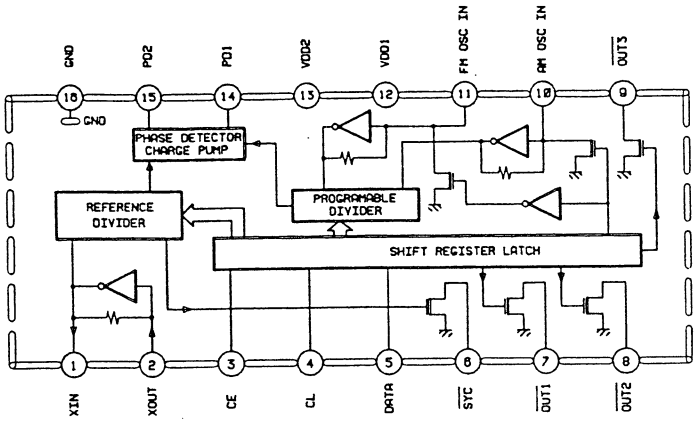
IC FUNCTION

PIN No.	SYMBOL	IN/OUT	DESCRIPTION
1	REMOT IN	I	REMOTE CONTROL INPUT
2	VCC	I	VDD CONNECTION
3	BACK UP/ CE	I	BACK UP MODE CONTROL
4, 94	TUNING UP / DOWN	I	TUNING UP TUNING DOWN 
5	TUNED	I	TUNED DISPLAY INPUT
6, 7, 9, 10	N.C		NO CONNECTION
11	RDS DATA	I	RDS DATA INPUT
8, 12~14	AREA OPTION	I	12, GROUND (EUROPE)
15, 20	N.C		NO CONNECTION
16~19	KEY IN	I	KEY MATRIX INPUT
21~23	KEY OUT	O	KEY MATRIX OUTPUT
24	N.C		NO CONNECTION
25	POWER	O	TUNER POWER ON
26	MUTE	O	MUTE OUTPUT
27	MONO/STEREO	O	MONO/STEREO SWITCHING OUTPUT
28~37	N.C		NO CONNECTIN
38	RESET	I	RESET IN
39	EXTAL	O	8.0MHz CRYSTAL U-COM OPERATOR
40	XTAL	I	
41	VSS		GROUND
42	TX	I	32.768KHz CRYSTAL TIME OPERATOR
43	TEX	O	
44, 45	N.C		NO CONNECTION
46	AVREF		+4.8V VDD
47	AVSS		ANALOG GROUND
48~70	S0~S22	O	FIP SEGMENT OUTPUT
71~74	N.C		NO CONNECTION
75~87	G13~G0	O	FIP GRIDE OUTPUT
88	VFIP	I	FIP VDD : -30V
89, 90	VDD	I	+4.8V VDD
91	VSS		GROUND
92, 93	N.C		NO CONNECTION
95	STEREO	I	STEREO INPUT
96	PLL-CK	O	PLL SERIAL CLOCK OUTPUT
97	PLL-DI	O	PLL SERIAL DATA OUTPUT
98	PLL-CE	O	PLL SERIAL CHIP ENABLE OUTPUT
99	REMOTE OUT	O	REMOTE CONTROL OUTPUT
100	RES CK	I	RDS CLOCK INPUT

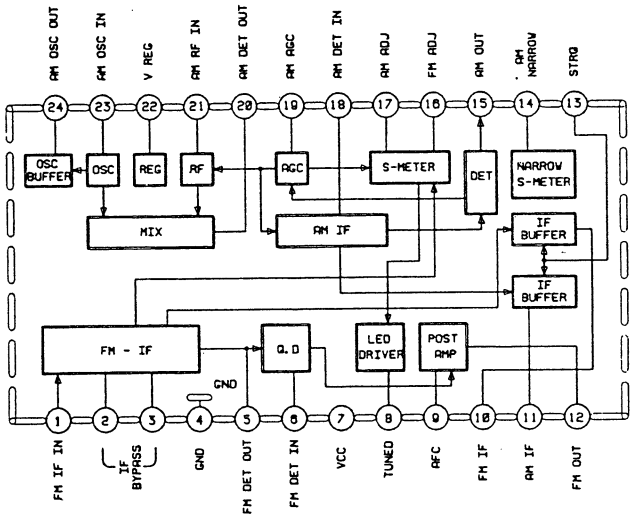

BVIANAM1177T
T7
T6
T5
T4
T3
T2
T1
T0
VFDP
VCC
NC
VSS
PC0/RTO0
PC1/RTO1
PC2/RTO2
PC3/RTO3
PC4
PC5
PC6
PC7
PE0/ECI0/INT0
PE1/ECI1/INT1
PE2/INT2
PE3/INT3/NMI
PE4/PWM
PE5/CTL
PE6/RMC
PE7/ROOT/ROOJ
PB0/CINT
PB1/CSI
PB2/SCK1
PB3/SI1
PB4/SO1
PB5/SCK1
PB6/SI1
PB7/SO1
PH0/XCK0
PH1/XRX0
PH2/XTX0
PH3/XCK1
PH4/XRX1
PH5/XTX1
PH6
PH7
PD0/S0
PD1/S1
PD2/S2
PD3/S3
PD4/S4
PD5/S5
PD6/S6
PD7/S7
PF0/S8
PF1/S9
PF2/S10
PF3/S11
PF4/S12
PF5/S13
PF6/S14
PF7/S15
PI0/S16
PI1/S17
PI2/S18
PI3/S19
PI4/S20
PI5/S21
PI6/S22
PI7/S23
T15/S24
T14/S25
T13/S26
T12/S27
T11/S28
T10/S29
T9/S30
T8/S31
PA7/AN7
PA6/AN6
TEX
TX
XTAL
EXTAL
RST
PA5/AN5
PA4/AN4
PA3/AN3
PA2/AN2
PA1/AN1
PA0/AN0
AVSS
AVREF


PA0/AN0 - PA7/AN7
A/D CONVERTER
T0-T7
T15/S24-T8/S31
P08/S8-P17/S23
VFDP
FDP CONTROLLER/ DRIVER
RAM
PE6/PWM
14 BIT PWM GENERATOR
PE5/CTL
PE7/DO8
CTL DUTY DET
PE5/RMC
REMOCON FIFO
PB1/CSB
PB3/SI8
PB4/SO8
PB2/SCK8
SERIAL INTERFACE UNIT 8
FIFO
PB6/SI1
PB7/SO1
PB5/SCK1
SERIAL INTERFACE UNIT 1
PE0/INT0/ECB
8 BIT TIMER/ COUNTER 8
8 BIT TIMER 1
PE7/TO
PB0/CINT
PE1/INT2/ECI
16 BIT CAPTURE TIMER/ COUNTER 2
PE7/ROJ
PE0/ECB/INT0
PE1/ECI/INT1
PE2/INT2
PE3/INT3/NMI
INTERRUPT CONTROLLER
SPC 700 CPU CORE
ROM 32K/48K BYTES
RAM 1120 BYTES
CLOCK GEN. SYSTEM CONTROL
PRESCALER/ TIMER BASE TIMER
32KHz TIMER/COUNTER
REALTIME PULSE GENERATOR
CH0
CH1
PC0/RTO0-PC3/RTO3
PORT A
PORT B
PORT C
PORT D
PORT E
PORT F
PORT G
PORT H
PORT I
P00-P07
P80-P86
P87
PC0-PC7
PD0-PD7
PE0-PE5
PE6, PE7
PF0-PF7
PG0-PG7
PH0-PH7
PI0-PI7

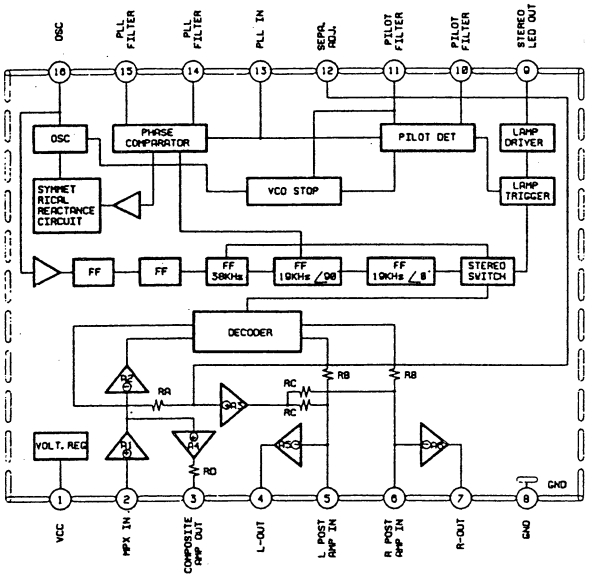
LM7001 PLL



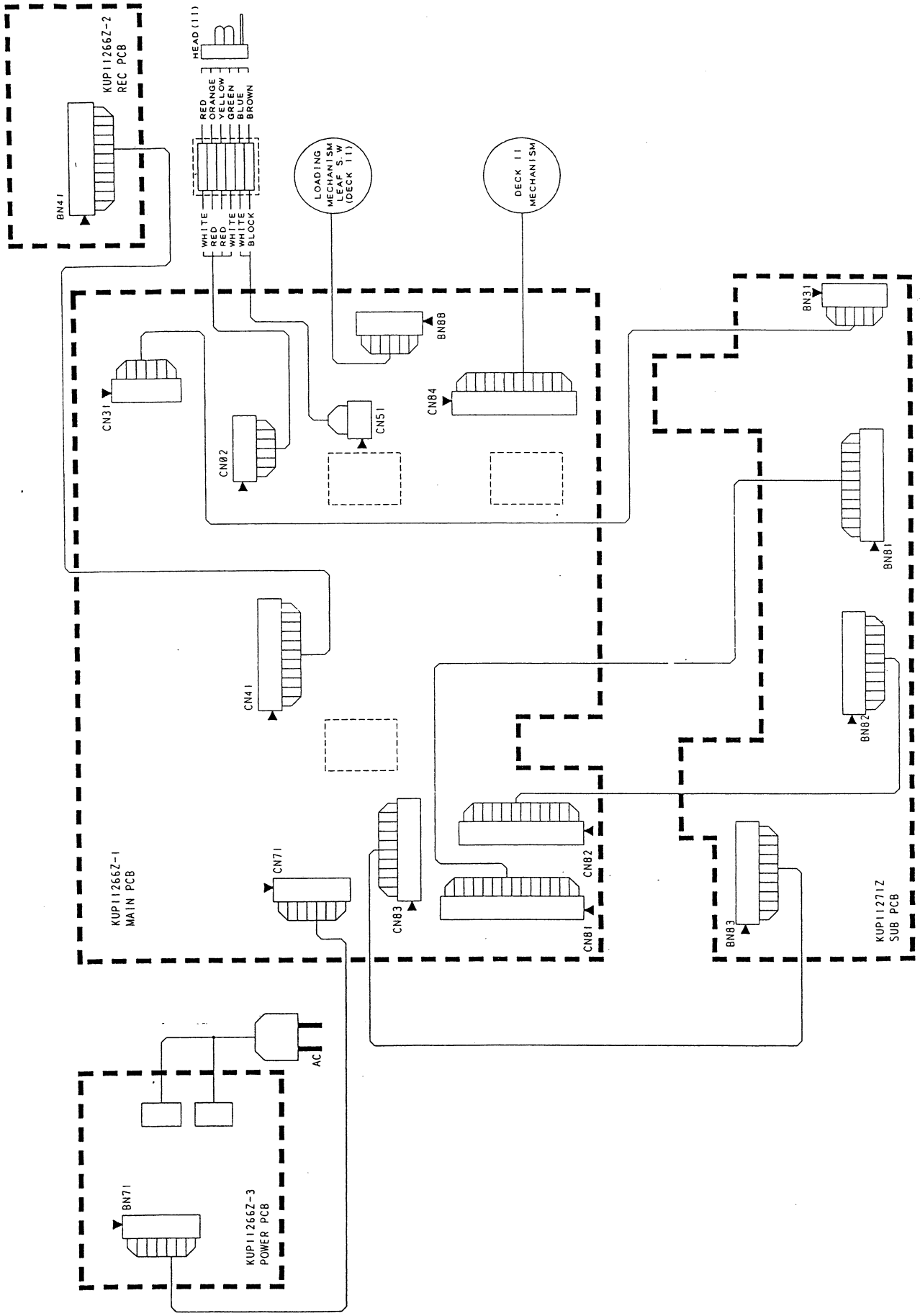
LA1266 FM IF & AM RF/IF



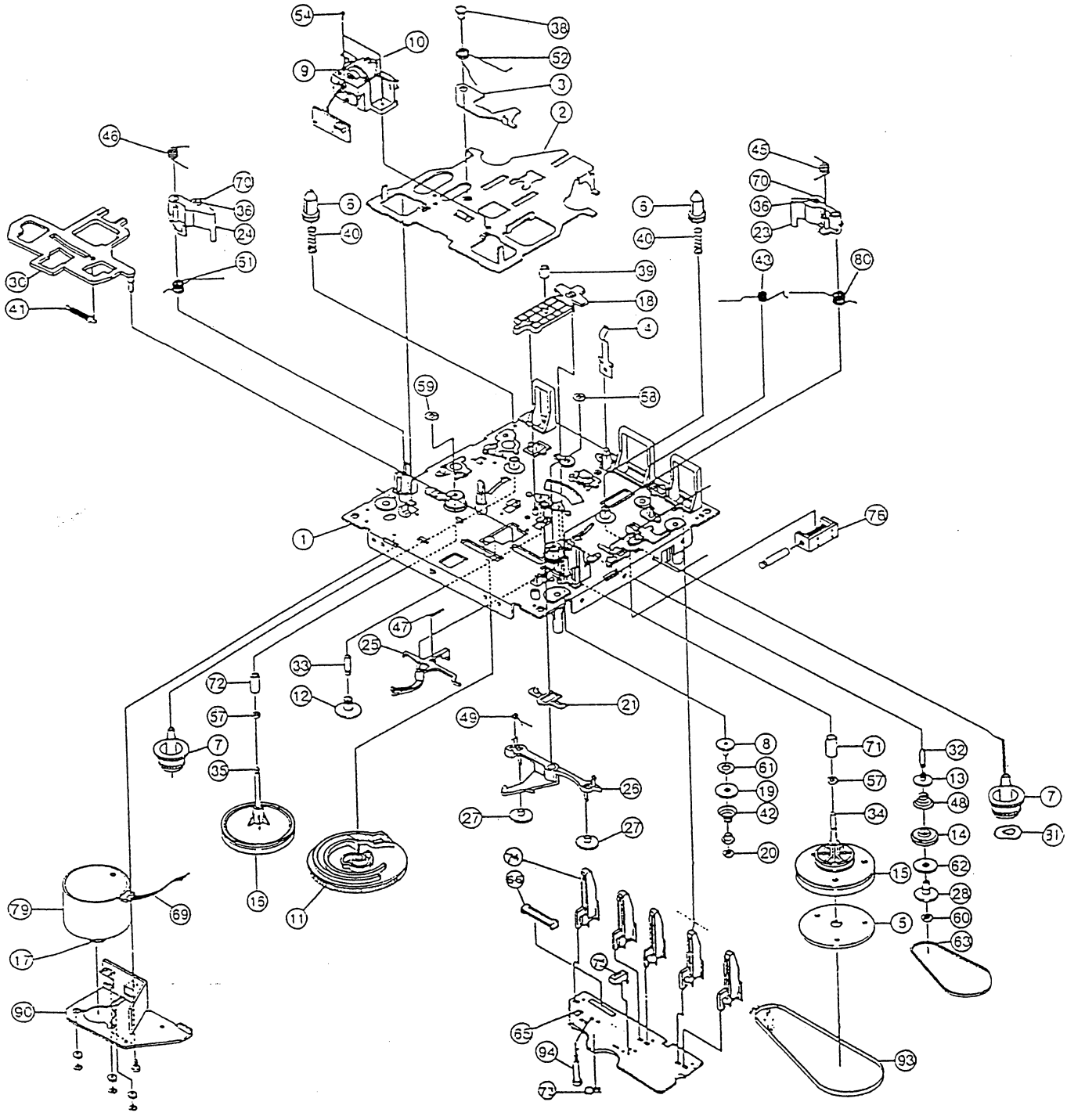
LA3410 MPX



WIRING DIAGRAM



MECHANISM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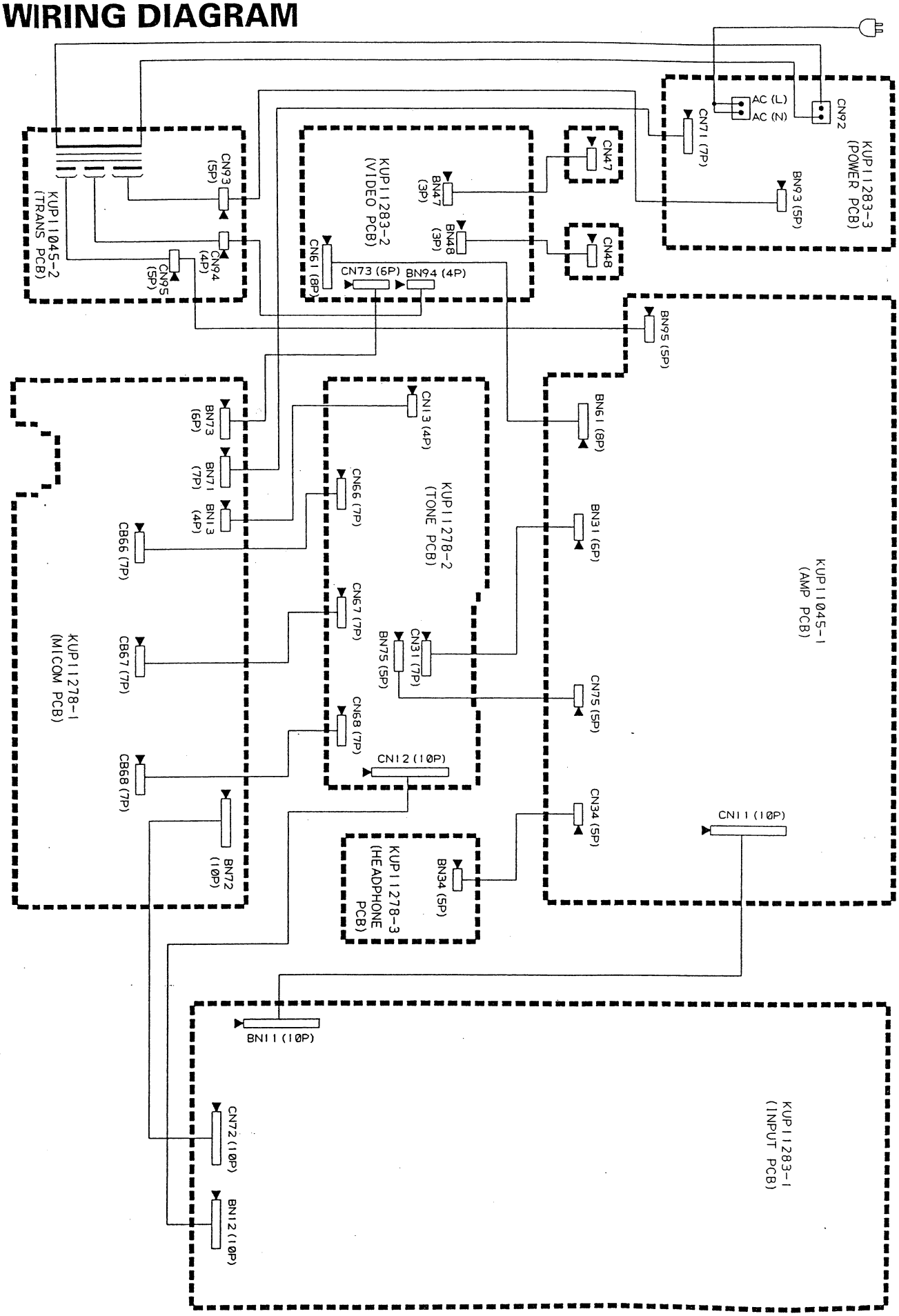
IC PIN FUNCTION (ANAM 1286M : NEC uPD 78P 0208GF)

PIN No.	SYMBOL	I/O	DESCRIPTION
1	VDD		POWER SUPPLY (+5V)
2	PWR ON H	O	WHEN "POWER ON" IS "H"
3~7	FUNC. INDICATOR	O	FUNCTION LED DRIVE OUTPUT
8	SURR ON/OFF	O	WHEN "SURROUND ON" IS "H"
9	POWER MUTE	O	HEADPHONE MUTE CONTROL OUTPUT
10	RESET	I	SYSTEM RESET INPUT
11,12	X OUT/IN	O/I	4.19MHz CRYSTAL CONNECTION TERMINAL
13	GND		GROUND
14	N/C		
15	PROTECT IN	I	INPUT FROM PROTECTION CIRCUIT
16	VDD		POWER SUPPLY (+5V)
17	STB	O	IC11 (NJU7312L) CONTROL OUTPUT
18	CLK	O	
19	DATA	O	
20	STB	O	IC21 (LA2786), IC22 (LV1015) CONTROL OUTPUT
21	CLK	O	
22	DATA	O	
23	CENTER MUTE	O	CENTER CHANNEL MUTE CONTROL OUTPUT
24	REAR MUTE	O	WHEN "SURROUND ON" IS "H"
25	GND		GROUND
26	AMP MUTE	O	SIGNAL MUTE CONTROL OUTPUT
27	POWER MUTE	O	SPEAKER CONTROL OUTPUT
28	-20dB MUTE	O	-20dB MUTE CONTROL OUTPUT
29,30	AC/BD	O	IC61 (BA7626) CONTROL OUTPUT
31	OPTION	I	V-4096 OPTION PORT
32,33	NC		
34	VDD		POWER SUPPLY (+5V)
35	VREF	I	REFERENCE VOLTAGE
36	BUS IN	I	SYSTEM CONTROL INPUT
37,42	MODE	I	REAR/CENTER/DELAY TIME UP/DN CONTROL INPUT
38,43	FUNCTION	I	FUNCTION SW UP/DN CONTROL INPUT
39	REMOTE IN	I	REMOTE CONTROL INPUT TERMINAL
40	GND		GROUND
41	BUS OUT	O	SYSTEM CONTROL OUTPUT
44,45	VR UP/DOWN	O	MASTER VOL. UP/DN CONTROL OUTPUT
46	VDD		POWER SUPPLY (+5V)
47~51	FIP	O	
52~56	KEY IN/OUT	O/I	KEY MATRIX INPUT/OUTPUT
57~62	FIP	O	GROUND
63~67	FIP	O	
68~78	FIP	O	SEGMENT
79	V LOAD	I	NEGATIVE POWER SUPPLY
80~90	FIP	O	SEGMENT
91~100	FIP	O	GRID

WIRING DIAGRAM



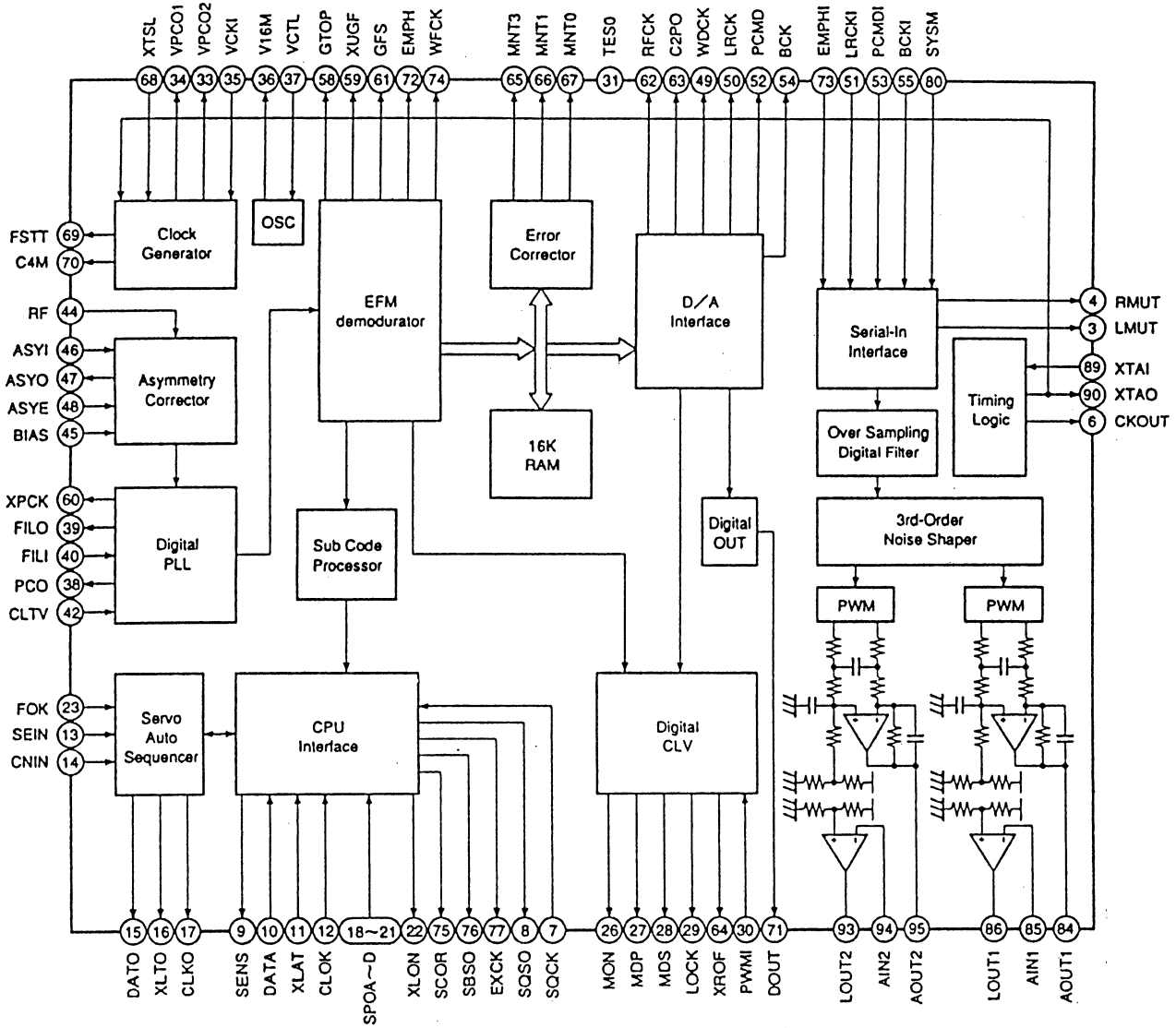
IC PIN FUNCTION

CXD2529Q (Digital Signal Processor)

NO.	SYMBOL	I/O		DESCRIPTION
1	V_{DD}	–	–	Power supply(+5V).
2	V_{SS}	–	–	GND.
3	LMUT	O	1,0	Left-channel zero detection flag.
4	RMUT	O	1,0	Right-channel zero detection flag.
5	TES2	O	1,0	TEST output pin; normally open.
6	CKOUT	O	1,0	Master clock frequency-divider output. Selects and outputs XTAI×1, × 1/2, × 1/4 or low only.
7	SQCK	I		SQSO readout clock input.
8	SQSO	O	1,0	Sub Q 80-bit serial output.
9	SENS	O	1,0	SENS output to CPU.
10	DATA	I		Serial data input from CPU.
11	XLAT	I		Latch input from CPU. Serial data is latched at the falling edge.
12	CLOK	I		Serial data transfer clock input from CPU.
13	SEIN	I		SENS input from SSP.
14	CNIN	I		Track jump count signal input.
15	DATO	O	1,0	Serial data output to SSP.
16	XLTO	O	1,0	Serial data latch output to SSP. Latched at the falling edge.
17	CLKO	O	1,0	Serial data transfer clock output to SSP.
18	SPOA	I		Microcomputer extended interface (input A).
19	SPOB	I		Microcomputer extended interface (input B).
20	SPOC	I		Microcomputer extended interface (input C).
21	SPOD	I		Microcomputer extended interface (input D).
22	XLON	O	1,0	Microcomputer extended interface (output).
23	FOK	I		Focus OK input. Used for SENS output and the servo auto sequencer.
24	V_{DD}	–	–	Power supply (+5V).
25	V_{SS}	–	–	GND.
26	MON	O	1,0	Spindle motor on/off control output.
27	MDP	O	1,Z,0	Spindle motor servo control.
28	MDS	O	1,Z,0	Spindle motor servo control.
29	LOCK	O	1,0	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low.
30	PWMI	I		Spindle motor external control input.
31	TES0	I		TEST pin; normally GND.
32	TES1	I		TEST pin; normally GND.
33	VPCO2	O	1,Z,0	Wide-band EFM PLL charge pump output. Turned on/off by FCSW of address E.
34	VPCO1	O	1,Z,0	Charge pump output for the wide-band EFM PLL.
35	VCKI	I		VCO2 oscillation input for the wide-band EFM PLL.
36	V16M	O	1,0	VCO2 oscillation output for the wide-band EFM PLL.
37	VCTL	I		VCO2 control voltage input for the wide-band EFM PLL.
38	PCO	O	1,Z,0	Master PLL charge pump output.
39	FILO	I	Analog	Master PLL (slave=digital PLL) filter output.
40	FILI	I		Master PLL filter input.
41	AV_{SS}	–	–	Analog GND.
42	CLTV	I		Master VCO control voltage input.
43	AV_{DD}	–	–	Analog power supply (+5V).
44	RF	I		EFM signal input.
45	BIAS	I		Constant current input of the asymmetry circuit.
46	ASYI	I		Asymmetry comparator voltage input.
47	ASYO	O	1,0	EFM full-swing output (low=Vss, high=V_{DD})
48	ASYE	I		Low: asymmetry circuit off; high: asymmetry circuit on.
49	WDCK	O	1,0	D/A interface. Word clock = 2fs.
50	LRCK	O	1,0	D/A interface. LR clock output f = fs.
51	LRCKI	I		LR clock input.

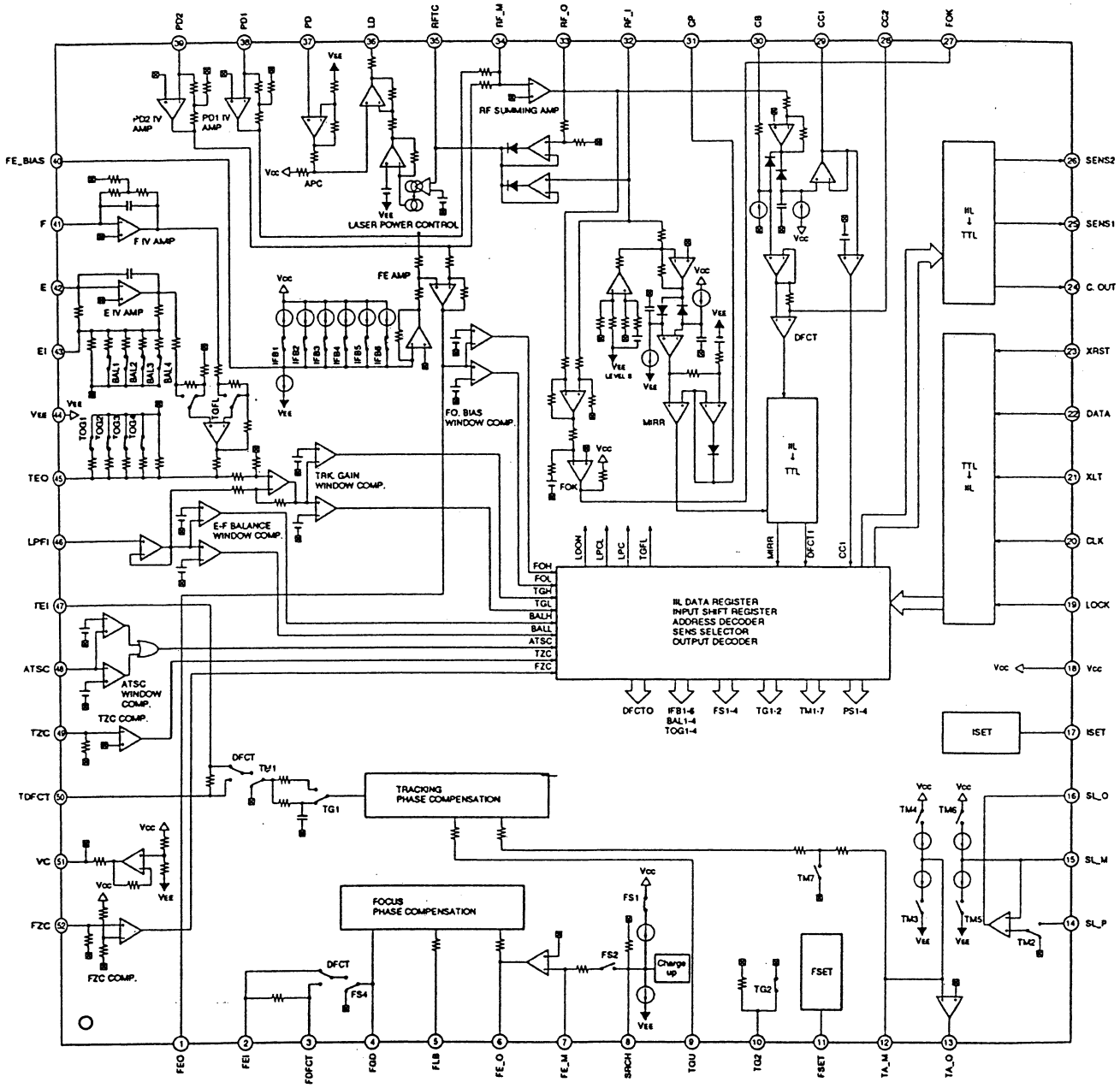
NO.	SYMBOL	I/O		DESCRIPTION
52	PCMD	O	1,0	D/A interface. Serial data output (two's complement, MSB first)
53	PCMDI	I		D/A interface. Serial data input (two's complement, MSB first)
54	BCK	O	1,0	D/A interface. Bit clock output.
55	BCKI	I		D/A interface. Bit clock input.
56	Vss	–	–	GND.
57	VDD	–	–	Power supply(+5V).
58	GTOP	O	1,0	GTOP output.
59	XUGF	O	1,0	XUGF output.
60	XPCK	O	1,0	XPLCK output.
61	GFS	O	1,0	GFS output.
62	RFCK	O	1,0	RFCK output.
63	C2PO	O	1,0	C2PO output.
64	XROF	O	1,0	XRAOF output.
65	MNT3	O	1,0	MNT3 output.
66	MNT1	O	1,0	MNT1 output.
67	MNT0	O	1,0	MNT0 output.
68	XTSL	I		Crystal selector input. Low: 16.9344MHz; high: 33.8688MHz.
69	FSTT	O	1,0	2/3 frequency-divider output for pins 89 and 90.
70	C4M	O	1,0	4.2336MHz output. 1/4 frequency-divided VCKI output in CAV-W mode.
71	DOUT	O	1,0	Digital Out output.
72	EMPH	O	1,0	Outputs a high signal when the playback disc has emphasis, and a low signal when there is no emphasis.
73	EMPHI	I		Inputs a high signal when de-emphasis is on, and a low signal when de-emphasis is off.
74	WFCK	O	1,0	WFCK output.
75	SCOR	O	1,0	Outputs a high signal when either subcode sync S0 or S1 is detected.
76	SBSO	O	1,0	Sub P to W serial output.
77	EXCK	I		SBSO readout clock input.
78	Vss	–	–	GND.
79	VDD	–	–	Power supply (+5V).
80	SYSM	I		Mute input. Active when high.
81	NC			
82	AVss	–	–	Analog GND.
83	AVDD	–	–	Analog power supply(+5V).
84	AOUT1	O		Left-channel analog output.
85	AIN1	I		Left-channel operational amplifier input.
86	LOUT1	O		Left-channel LINE output.
87	AVss	–	–	Analog GND.
88	XVDD			Power supply for master clock.
89	XTAI	I		Crystal oscillation circuit input. Input the external master clock via this pin.
90	XTAO	O		Crystal oscillation circuit output.
91	XVss			GND for master clock.
92	AVss	–	–	Analog GND.
93	LOUT2	O		Right-channel LINE output.
94	AIN2	I		Right-channel operational amplifier input.
95	AOUT2	O		Right-channel analog output.
96	AVDD	–	–	Analog power supply(+5V).
97	AVss	–	–	Analog GND.
98	NC			
99	NC			
100	XRST	I		System reset. Reset when low.

Notes)
- PCMD is an MSB first, two' s complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protecton window released)
- XUGF is the negative pulse for the frame sync derived from the EFM signal. It is the signal before sync protec tion.
- XPLCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge of XPLCK and the EFM signal transition point coincide.
- GFS goes high when the frame sync and the insertion protection timing match.
- RFCK is derived with the crystal accuracy. This signal has a cycle of 136μs (during normal-speed).
- C2PO represents the data error status.
- XRAOF is generated when the 16K RAM exceeds the $\pm$4F jitter margin.


XTSL 68
VPCO1 34
VPCO2 33
VCKI 35
V16M 36
VCTL 37
GTOP 58
XUGF 59
GFS 61
EMPH 72
WFCK 74
MNT3 65
MNT1 66
MNT0 67
TES0 31
RFCK 62
C2PO 63
WDCK 49
LRCK 50
PCMD 52
BCK 54
EMPHI 73
LRCKI 51
PCMDI 53
BCKI 55
SYSM 80
FSTT 69
C4M 70
RF 44
ASYI 46
ASYO 47
ASYE 48
BIAS 45
XPCK 60
FILO 39
FILI 40
PCO 38
CLTV 42
FOK 23
SEIN 13
CNIN 14
Clock Generator
OSC
EFM demodurator
Error Corrector
D/A Interface
Serial-In Interface
Timing Logic
Asymmetry Corrector
16K RAM
Over Sampling Digital Filter
Digital PLL
Sub Code Processor
Digital OUT
3rd-Order Noise Shaper
PWM
PWM
Servo Auto Sequencer
CPU Interface
Digital CLV
4 RMUT
3 LMUT
89 XTAI
90 XTAO
6 CKOUT
15 DATO
16 XLTO
17 CLKO
9 SENS
10 DATA
11 XLAT
12 CLOK
18~21 SPOA~D
22 XLON
75 SCOR
76 SBSO
77 EXCK
8 SQSO
7 SQCK
26 MON
27 MDP
28 MDS
29 LOCK
64 XROF
30 PWMI
71 DOUT
93 LOUT2
94 AIN2
95 AOUT2
86 LOUT1
85 AIN1
84 AOUT1

CXA1992BR (RF AMP+Servo signal processor)

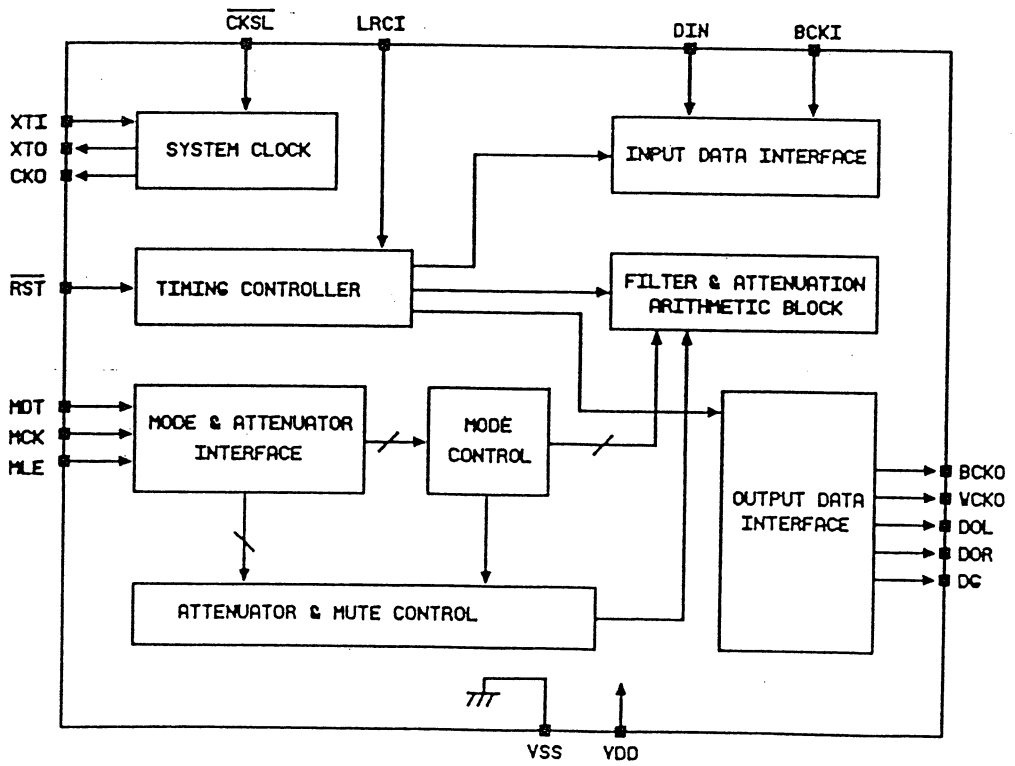
NO.	SYMBOL	I/O	DESCRIPTION
1	FEO	O	Focus error amplifier output. Connected internally to the window comparator input for bias adjustment.
2	FEI	I	Focus error input.
3	FDFCT	I	Capacitor connection pin for defect time constant.
4	FGD	I	Ground this pin through a capacitor for cutting the focus servo high-frequency gain.
5	FLB	I	External time constant setting pin for boosting the focus servo low-frequency.
6	FE-O	O	Focus drive output.
13	TA-O	O	Tracking drive output.
16	SL-O	O	Sled drive output.
7	FE-M	I	Focus amplifier inverted input.
8	SRCH	I	External time constant setting pin for generating focus search waveform.
9	TGU	I	External time constant setting pin for switching tracking high-frequency gain.
10	TG2	I	External time constant setting pin for switching tracking high-frequency gain.
11	FSET	I	Peak frequency setting pin for focus and tracking phase compensation amplifier.
12	TA-M	I	Tracking amplifier inverted input.
14	SL-P	I	Sled amplifier non-inverted input.
15	SL-M	I	Sled amplifier inverted input.
17	ISET	I I	Connect an external capacitance to set the current which determines the Focus search, Track jump, and Sled kick heights.
18	Vcc	I	Positive power supply.
19	LOCK	I	The sled overrun prevention circuit operates when this pin is low.(no pull-up resistance)
20	CLK	I	Serial data transfer clock input from CPU. (no-pull-up resistance)
21	DATA	I	Serial data input from CPU.(no pull-up resistance)
22	XLT	I	Latch input from CPU.(no pull-up resistance)
23	XRST	I	Reset input; resets at Low.(no pull-up resistance)
24	C. OUT	O	Track number count signal output.
25	SENS1	O	Outputs FZC, DFCT1, TZC, BALH, TGH, FOH, ATSC, and others according to the command from CPU.
26	SENS2	O	Outputs DFCT2,MIRR,BALL,TGL,FOL, and others according to the command from the CPU.
27	FOK	O	Focus OK comparator output.
28	CC2	I	Input for the defect bottom hold output with capacitance coupled.
29	CC1	O	Defecct bottom hold output. Connected internally to the interruption comparator input.
30	CB	I	Connection pin for defect bottom hold capacitor.
31	CP	I	Connection pin for MIRR hold capacitor. MIRR comparator non-inverted input.
32	RF-I	I	Input for the RF summing amplifier output with capacitance coupled.
33	RF-O	O	RF summing amplifier output. Eyepattern check point.
34	RF-M	I	RF summing amplifier inverted input. The RF amplifier gain is determined by the resistance connected between this pin and RFO pin.
35	RFTC	I	External time constant setting pin durring RF level control.
36	LD	O	APC amplifier output.
37	PD	I	APC amplifier input.
38	PD1	I	REI-V amplifier inverted input.
39	PD2	I	Connect these pins to the photo diode A+C and B+D pins.
40	FE-BIAS	I	Bias adjustment of focus error amplifier. Leave this pin open for automatic adjustment.
41	F	I	FI-V and EI-V amplifier inverted input.
42	E	I	Connect these pins to photo diode F and E.
43	EI	–	I-V amplifier E gain adjustment. (When not using automatic balance adjustment)
44	VEE	–	Negative power supply.
45	TEO	O	Tracking error amplifier output. E-F signal is output.
46	LPFI	I	Comparator input for balance adjustment. (input from TEO through LPF)
47	TEI	I	Tracking error input.
48	TDFCT	I	Capacitor connection pin for defect time constant.
49	ATSC	I	Window comparator input for ATSC detection.
50	TZC	I	Tracking zero-cross comparator input.
51	VC	O	(Vcc+VEE)/2 direct voltage output.
52	FZC	I	Focus zero-cross comparator input.


PD2
PD1
PD
LD
RFTC
RF_M
RF_O
RF_I
CP
CB
CC1
CC2
FOK
PD2 IV AMP
PD1 IV AMP
RF SUMMING AMP
APC
LASER POWER CONTROL
FE_BIAS
F
F IV AMP
E
E IV AMP
EI
FE AMP
FO. BIAS WINDOW COMP.
DFCT
MIRR
IIL → TTL
TTL → IIL
SENS2
SENS1
C. OUT
XRST
DATA
XLT
CLK
LOCK
TEO
TRK. GAIN WINDOW COMP.
E-F BALANCE WINDOW COMP.
LPFI
TEI
ATSC
ATSC WINDOW COMP.
TZC COMP.
TZC
IIL DATA REGISTER
INPUT SHIFT REGISTER
ADDRESS DECODER
SENS SELECTOR
OUTPUT DECODER
DFCTO
IFB1-6 BAL1-4 TOG1-4
FS1-4
TG1-2
TM1-7
PS1-4
ISET
TDFCT
TRACKING PHASE COMPENSATION
VC
FZC
FZC COMP.
FOCUS PHASE COMPENSATION
Charge up
FSET
TM4
TM6
TM3
TM5
TM7
SL_O
SL_M
SL_P
FEO
FEI
FDFCT
FGD
FLB
FE_O
FE_M
SRCH
TGU
TG2
TA_M
TA_O

SM5841AP (Digital filter)

NO.	SYMBOL	I/O	DESCRIPTION
1	$\overline{CKLS}$	IP	Oscillator and input frequency select. 384fs when HIGH, and 256fs when LOW.
2	XTI	I	Oscillator input connection.
3	XTO	O	Oscillator output connection.
4	CKO	O	Oscillator output clock (same frequency as XTI).
5	VSS	—	Ground
6	MDT	IP	Digital attenuator and mode set data .
7	$\overline{MCK}$	IP	Digital attenuator and mode set clock.
8	MLE	IP	Digital attenuator and mode set latch enable.
9	$\overline{RST}$	IP	System Reset.
10	DG	O	8fs left/right simultaneous of 4fs left/right alternating de-glitched output.
11	DOR	O	Right-channel data output when in 8fs L/R simultaneous mode, and L/R clock output in 4fs L/R alternating mode.
12	DOL	O	Left-channel data output when in 8fs L/R simultaneous mode, and Left/Right channel data output in L/R alternating mode.
13	WCKO	O	Output word clock.
14	VDD	—	5V supply.
15	BCKO	O	Output bit clock.
16	LRCI	IP	Input data sample rate (fs) clock.
17	BCKI	IP	Input bit clock.
18	DIN	IP	Data input.

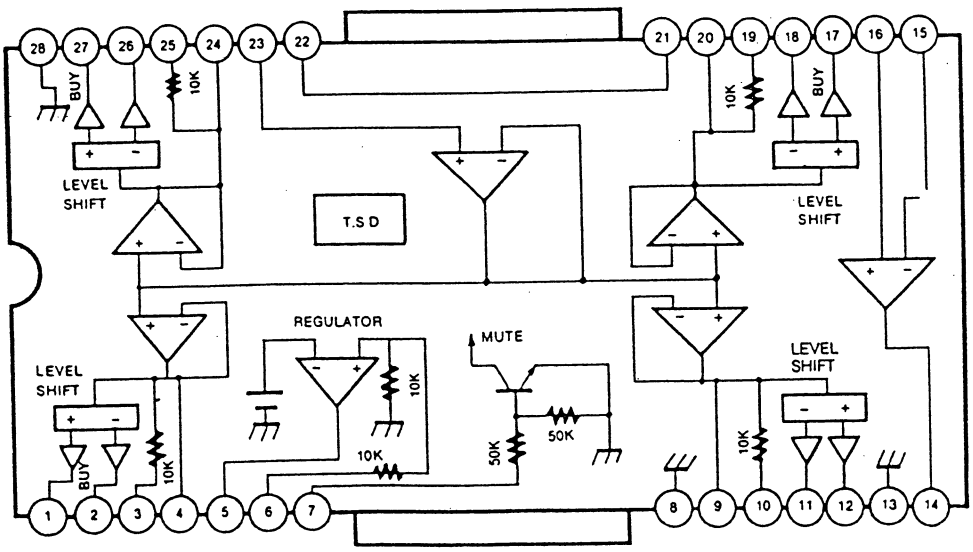
BLOCK DIAGRAM



KA9258D (Motor Driver)

NO.	SYMBOL	I/O	DESCRIPTION
1	DO1.1	O	DRIVE OUTPUT
2	DO1.2	O	DRIVE OUTPUT
3	DI1.1	I	DRIVE INPUT
4	DI1.2	I	DRIVE INPUT
5	REG	–	REGULATOR
6	REO	O	REGULATOR OUTPUT
7	MUTE	–	MUTE
8	GND1	–	GROUND
9	DI2.1	I	DRIVE INPUT
10	DI2.2	I	DRIVE INPUT
11	DO2.1	O	DRIVE OUTPUT
12	DO2.2	O	DRIVE OUTPUT
13	GND2	–	GROUND
14	OPOUT	O	OPAMP OUTPUT
15	OPIN (-)	I	OPAMP INPUT(-)
16	OPIN (+)	I	OPAMP INPUT(+)
17	DO3.1	O	DRIVE OUTPUT
18	DO3.2	O	DRIVE OUTPUT
19	DI3.1	I	DRIVE INPUT
20	DI3.2	I	DRIVE INPUT
21	VCC1	–	SUPPLY VOLTAGE
22	VCC2	–	SUPPLY VOLTAGE
23	VREF	–	2.5V BIAS VOLTAGE
24	DI4.1	I	DRIVE INPUT
25	DI4.2	I	DRIVE INPUT
26	DO4.1	O	DRIVE OUTPUT
27	DO4.2	O	DRIVE OUTPUT
28	GND3	–	GROUND

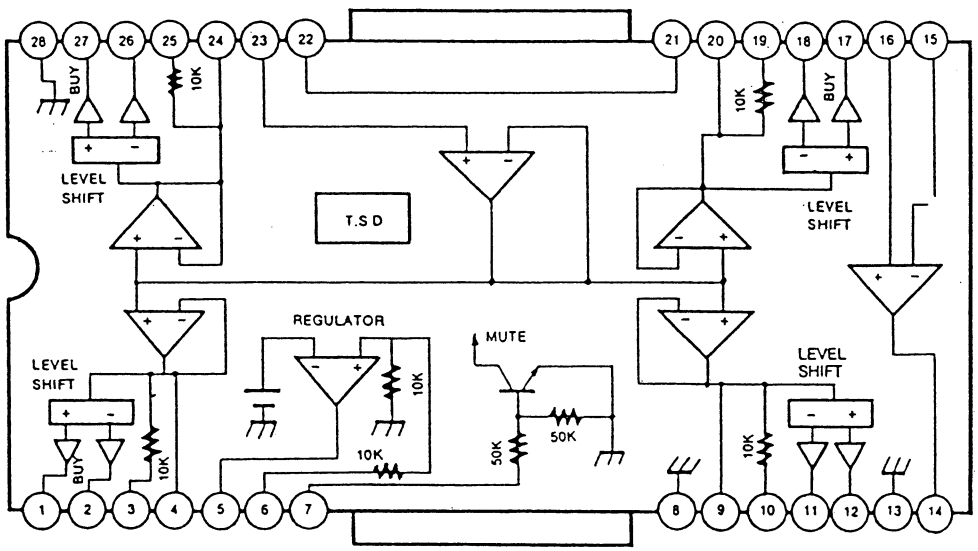
BLOCK DIAGRAM



KA9258D (Motor Driver)

NO.	SYMBOL	I/O	DESCRIPTION
1	DO1.1	O	DRIVE OUTPUT
2	DO1.2	O	DRIVE OUTPUT
3	DI1.1	I	DRIVE INPUT
4	DI1.2	I	DRIVE INPUT
5	REG	–	REGULATOR
6	REO	O	REGULATOR OUTPUT
7	MUTE	–	MUTE
8	GND1	–	GROUND
9	DI2.1	I	DRIVE INPUT
10	DI2.2	I	DRIVE INPUT
11	DO2.1	O	DRIVE OUTPUT
12	DO2.2	O	DRIVE OUTPUT
13	GND2	–	GROUND
14	OPOUT	O	OPAMP OUTPUT
15	OPIN (-)	I	OPAMP INPUT(-)
16	OPIN (+)	I	OPAMP INPUT(+)
17	DO3.1	O	DRIVE OUTPUT
18	DO3.2	O	DRIVE OUTPUT
19	DI3.1	I	DRIVE INPUT
20	DI3.2	I	DRIVE INPUT
21	VCC1	–	SUPPLY VOLTAGE
22	VCC2	–	SUPPLY VOLTAGE
23	VREF	–	2.5V BIAS VOLTAGE
24	DI4.1	I	DRIVE INPUT
25	DI4.2	I	DRIVE INPUT
26	DO4.1	O	DRIVE OUTPUT
27	DO4.2	O	DRIVE OUTPUT
28	GND3	–	GROUND

BLOCK DIAGRAM



IC70 BVIANAM1232C (μ-COM, TMP87PM78F)

NO.	SYMBOL	I/O	DESCRIPTION
1	VDD	-	+5V POWER SUPPLY PIN
2	F_MOTOR	O	MESHANISM OPEN CONTROL OUTPUT PIN
3	R_MOTOR	O	MESHANISM CLOSE CONTROL OUTPUT PIN
4	/MLE	O	DIGITAL ATTENUATOR AND MODE SET LATCH ENABLE
5	MCK	O	DIGITAL ATTENUATOR AND MODE SET CLOCK
6	MDT	O	DIGITAL ATTENUATOR AND MODE SET DATA
7	REMO SEL	I	REMOTE SELECTOR SWITCH CHECK PIN
8	TEST	I	OPTION(HIGH=AKAI)
9	NC	-	
10	SQCK	O	SUBCODE-Q DATA CLOCK OUTPUT PIN
11	SQSO	I	SUBCODE-Q DATA SERIAL INPUT PIN
12	NC	-	
13	SCOR	I	SUBCODE SYNC SIGNAL (S0+S1) INPUT PIN
14	OP/SW	I	OPEN SWITCH CHECK INPUT PIN
15	CL/SW	I	CLOSE SWITCH CHECK INPUT PIN
16	JOG B	-	SKIP DIAL CONTROL PIN
17	JOG A	-	SKIP DIAL CONTROL PIN
18~21	NC,	-	
22	GND	-	GROUND
23	AGND	-	GROUND
24	VREF	-	+5V POWER SUPPLY PIN
25	VDD	-	+5V POWER SUPPLY PIN
26	NC	-	
27	GND	-	GROUND
28, 29	NC	-	
30	GND	-	GROUND
31	XIN	I	SYSTEM CLOCK OSCILLATION CRYSTAL INTERFACE INPUT PIN
32	XOUT	O	SYSTEM CLOCK OSCILLATION CRYSTAL INTERFACE OUTPUT PIN
33	RESET	I	SYSTEM RESET PIN
34	RE_IN	I	REMOCON DATA INPUT PIN
35	BUS_IN	I	REMOCON DATA INPUT PIN
36	BUS_OUT	O	REMOCON DATA OUTPUT PIN
37	SENS2	I	SSP STATUS INPUT PIN
38	SENS	I	DSP STATUS INPUT PIN
39	COUT	I	TRACK COUNT INPUT PIN
40	MUTE	O	AUDIO MUTE OUTPUT PIN
41	CLOCK	O	CLOCK OUTPUT PIN
42	XLAT	O	LATCH OUTPUT PIN
43	DATA	O	DATA OUTPUT PIN
44	F.OK	I	FOCUS OK INPUT PIN
45	GFS	I	FRAME SYNC STAUS INPUT PIN
46	DSP RESET	O	SYSTEM RESET FROM DSP OUTPUT PIN
47	POWER	O	SYSTME POWER ON/OFF OUTPUT PIN
48	FLT POWER	O	FIP FILAMENT POWER ON, OFF OUTPUT PIN

NO.	SYMBOL	I/O	DESCRIPTION
49	NC	-	
50	-30V	-	FIP VOLTAGE SUPPLY PIN
51	LED	O	STANBY LED ON/OFF OUTPUT PIN
52	LED	O	TIME EDIT LED ON/OFF OUTPUT PIN
53	LED	O	JUST EDIT LED ON/OFF OUTPUT PIN
54	LED	O	MANUAL FADE LED ON/OFF OUTPUT PIN
55	LED	O	AUTO SPACE LED ON/OFF OUTPUT PIN
56~58	NC	-	
59	KS_1	O	KEY SCAN OUTPUT PIN
60	KS_2	O	KEY SCAN OUTPUT PIN
61	KS_3	O	KEY SCAN OUTPUT PIN
62	KS_4	O	KEY SCAN OUTPUT PIN
63	KS_5	O	KEY SCAN OUTPUT PIN
64	KS_6	O	KEY SCAN OUTPUT PIN (NOT USED)
65	KS_7	O	KEY SCAN OUTPUT PIN (NOT USED)
66	KS_8	O	KEY SCAN OUTPUT PIN (NOT USED)
67	P1	O	FIP SEGEMENT SIGNAL OUTPUT PIN
68	P2	O	FIP SEGEMENT SIGNAL OUTPUT PIN
69	P3	O	FIP SEGEMENT SIGNAL OUTPUT PIN
70	P4	O	FIP SEGEMENT SIGNAL OUTPUT PIN
71	P5	O	FIP SEGEMENT SIGNAL OUTPUT PIN
72	P6	O	FIP SEGEMENT SIGNAL OUTPUT PIN
73	P7	O	FIP SEGEMENT SIGNAL OUTPUT PIN
74	P8	O	FIP SEGEMENT SIGNAL OUTPUT PIN
75	P9	O	FIP SEGEMENT SIGNAL OUTPUT PIN
76	P10	O	FIP SEGEMENT SIGNAL OUTPUT PIN
77	P11	O	FIP SEGEMENT SIGNAL OUTPUT PIN
78	P12	O	FIP SEGEMENT SIGNAL OUTPUT PIN
79	P13	O	FIP SEGEMENT SIGNAL OUTPUT PIN
80	P14	O	FIP SEGEMENT SIGNAL OUTPUT PIN
81	P15	O	FIP SEGEMENT SIGNAL OUTPUT PIN
82	P16	O	FIP SEGEMENT SIGNAL OUTPUT PIN
83	1G	O	FIP TIMING SIGNAL OUTPUT PIN
84	2G	O	FIP TIMING SIGNAL OUTPUT PIN
85	3G	O	FIP TIMING SIGNAL OUTPUT PIN
86	4G	O	FIP TIMING SIGNAL OUTPUT PIN
87	5G	O	FIP TIMING SIGNAL OUTPUT PIN
88	6G	O	FIP TIMING SIGNAL OUTPUT PIN
89	7G	O	FIP TIMING SIGNAL OUTPUT PIN
90	8G	O	FIP TIMING SIGNAL OUTPUT PIN
91~94	GND	I	GROUND
95	KI_4	I	KEY SCAN INPUT PIN
96	KI_3	I	KEY SCAN INPUT PIN
97	KI_2	I	KEY SCAN INPUT PIN
98	KI_1	I	KEY SCAN INPUT PIN
99	P17	O	FIP SEGMENT SIGNAL OUTPUT PIN
100	NC	-	

MEASUREMENT AND ADJUSTMENT METHODS

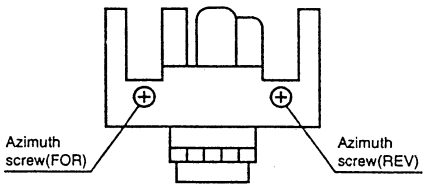
Measurement condition
- Dolby NR position: OFF
- Make sure heads are clean
- Make sure capstan and pressure roller are clean.

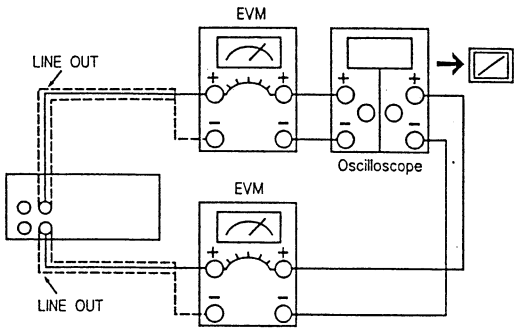
MEASURING INSTRUMENTS
- EVM (Electronic Voltmeter)
- Oscilloscope
- Frequency counter
- AF Oscillator
- DC Voltmeter
- ATT (Attenuator)
- Resistor (600Ω)

Test tape
- Head azimuth (10KHz, -10dB): MTT-114N
- Tape speed(3KHz, -10dB): MTT-111N
- Playback frequency response MTT-257H (125KHz, 1KHz, 10KHz, -10dB)
- Playback gain: MTT-150
- Blank tape
  Normal blank tape: MTT-5513
  CrO_2 blank tape: MTT-5563
  Metal blank tape: MTT-5572

HEAD AZIMUTH ADJUSTMENT

1. Test equipment connections are shown in fig. 1.
2. Playback the head Azimuth test tape and regulate the angle adjust screw so that the outputs of L-ch and R-ch are maximized. (When the adjusting positions are different with L-ch and R-ch, find a position where the outputs of L-ch and R-ch are balanced and then make the adjustment.)
3. At the same time, obtain a lissajous waveform and eliminate phase deflection.
4. After the adjustment, apply screw lock to the angle adjusting value.



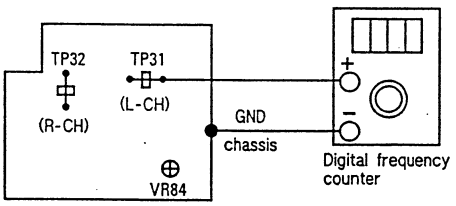


(FIG. 1)

TAPE SPEED ADJUSTMENT

1. Test equipment connections are shown in fig. 2.
2. Playback the middle part of the test tape.

Adjustment point	VR84
Standard Value	3,000Hz ± 30Hz

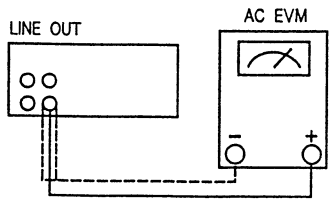


(FIG. 2)

PLAYBACK GAIN ADJUSTMENT

1. Test equipment connections are shown in fig. 3.
2. Playback the playback gain test tape. (MTT-150).
3. Adjust playback gain.

Adjustment Point	L ch : VR01	R ch : VR02
Standard Value	560mV	

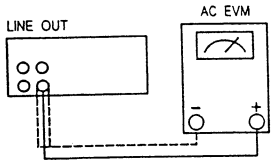


(FIG. 3)

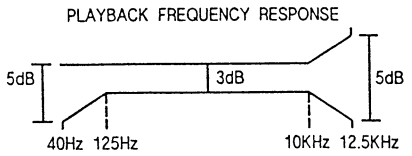
DECK

PLAYBACK FREQUENCY RESPONSE

1. Testequipment connections are shown in fig. 4.
2. Playback the playback frequency response test tape.
3. Check that the frequency response is within the range shown in Fig. 5 for both L-ch and R-ch.



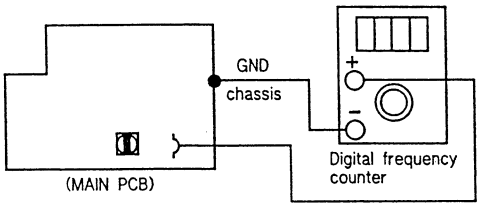
(FIG. 4)



(FIG. 5)

BIAS FREQUENCY ADJUSTMENT

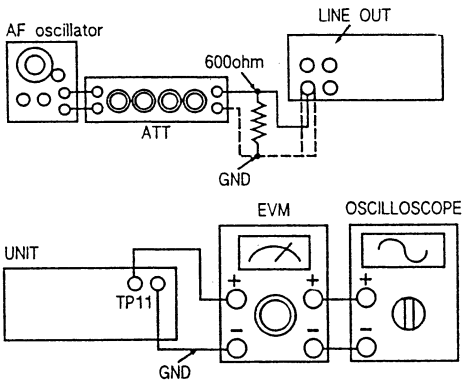
1. Test equipment connections are shown in fig. 6.
2. Load a CrO_2 blank test tape.
3. Press the record and pause button.
4. Adjust T501 for 105KHz frequency counter reading.



(FIG. 6)

OVERALL GAIN ADJUSTMENT

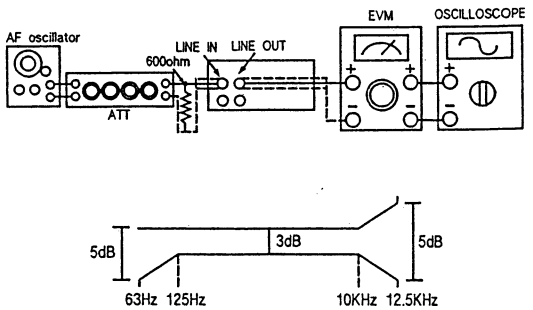
1. Test equipment connections are shown in fig. 7.
2. Insert the normal reference blank tape.
3. Place UNIT into recorde mode.
4. Supply a 1KHz signal through ATT (-10dB) from AF oscillator to line in.
5. Adjust ATT until monitor level at TP31 (L-ch) or TP32 (R-ch) becomes 180mV.
6. Playback recorded tape and make sure that the output level at TP31 (L-ch) or TP32 (R-ch) becomes 180mV.
7. If measured value is not 180mV, adjust it by using VR31 (L-CH) or VR32 (R-CH).
8. Repeat from step (2).



(FIG. 7)

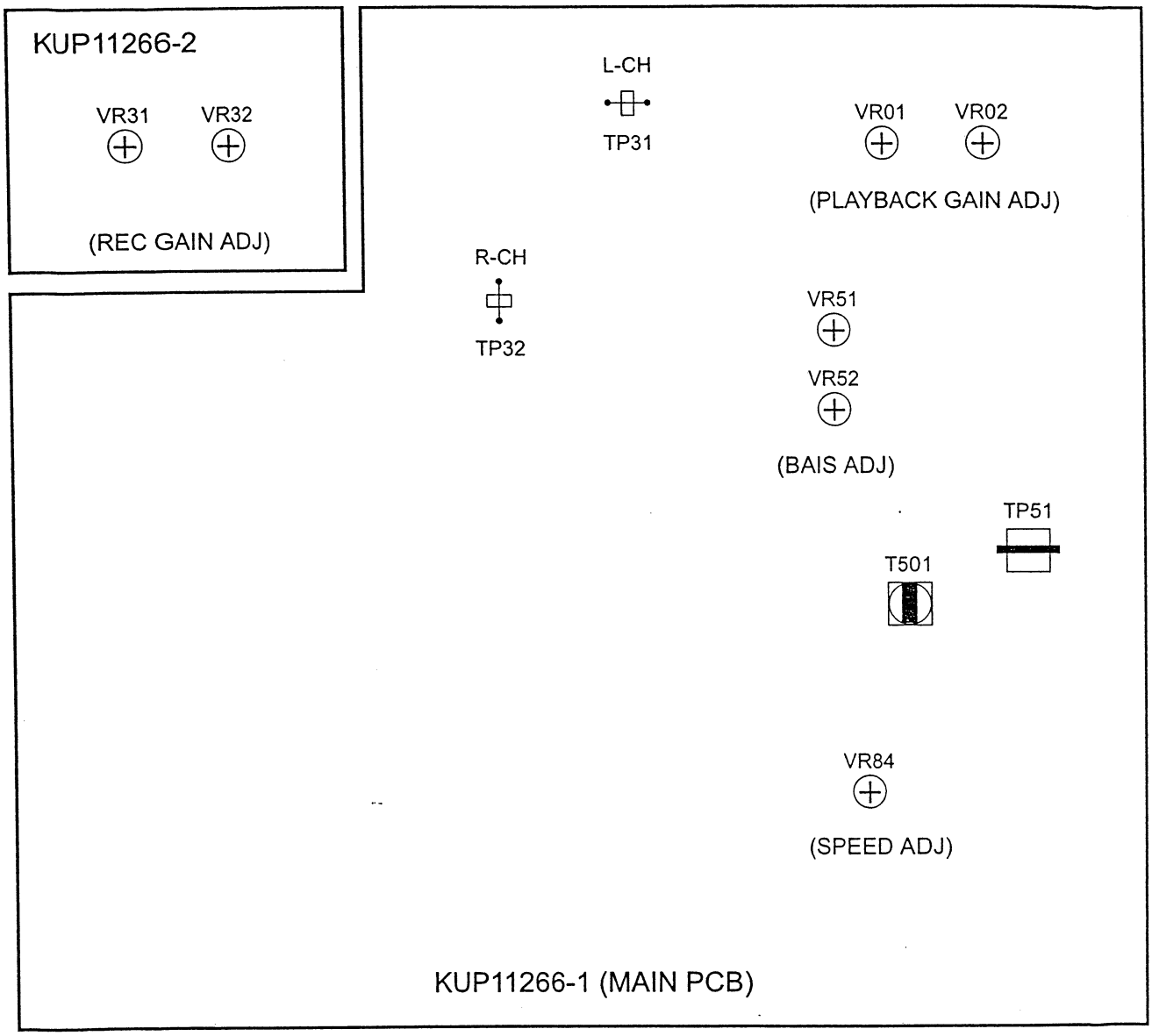
OVERALL FREQUENCY RESPONSE

1. Set a normal blank tape (MTT-5513) and record by apply signal (100Hz, 1KHz, 10KHz) through ATT-from AF oscillator to line in (Line out Level : 33mV).
2. Playback the signal recorded in step 1, and check that the level of each output frequency in within the range shown in fig. 8 in comparison with the reference frequency (1KHz).
3. If it is not within the standard range adjust the bias current by using VR51 (L-CH) or VR52 (R-CH) so that the frequency level is within the standard.
   - Level up in high frequency range ... Increase the bias current.
   - Level down in high frequency range ... Decrease the bias current.
4. After that. increase the signal recorded on CrO_2 blank tape (MTT-5563) and metal blank tape (MTT-5572) up to 12KHz and adjust in the same way as mentioned above and check that the frequency level is within the range shown in Fig. 8.



(FIG. 8)

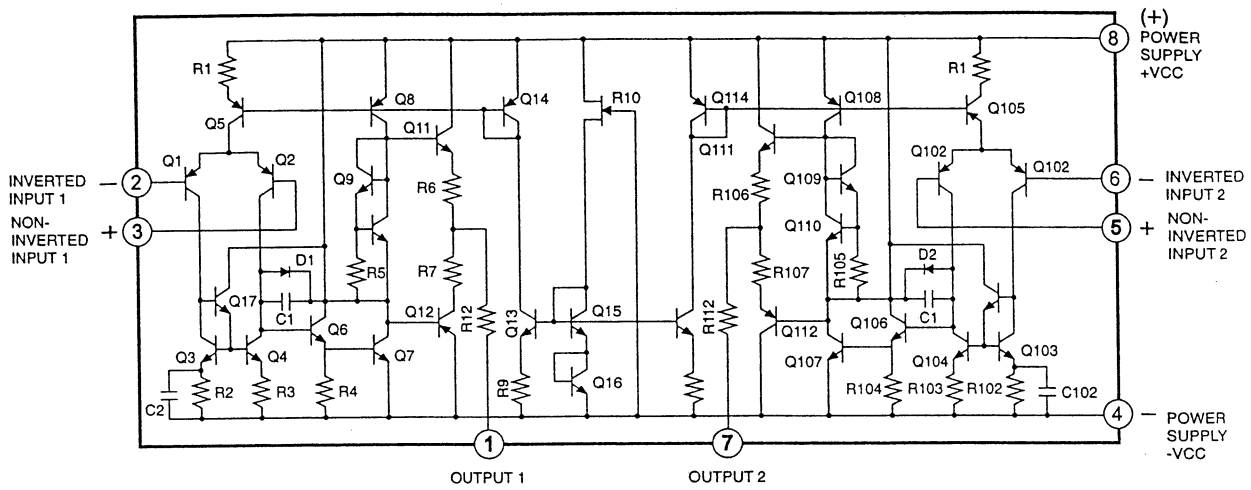
ADJUSTMENT POINT



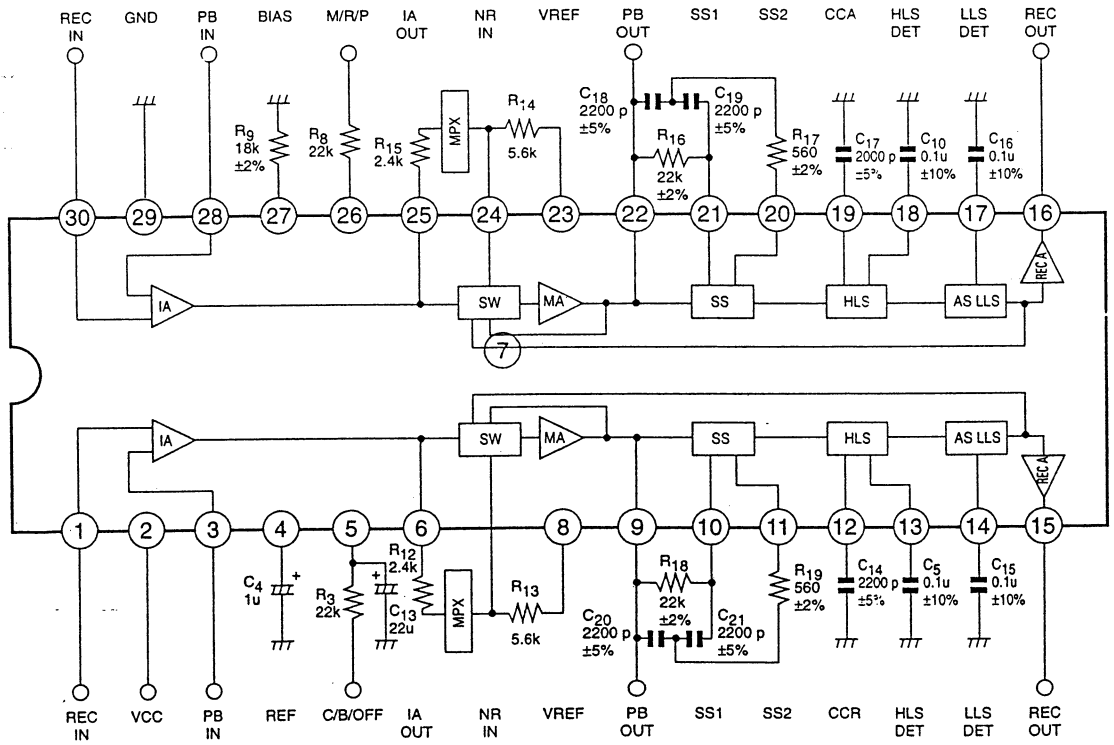
μ-COM IC (ANAM1265D)(UPD78042GF)

PIN No.	SYMBOL	DESCRIPTION
3~7	SEG~SEG1	FIP digit select output for indication.
8	VDD	+5V Power supply terminal of this IC.
14~16	Key OUT	Key scan output.
17	$\overline{\text{RESET}}$	System reset pluse input.
18~19	TIME	Timer control Mode.
20	GND	To be grounded.
21~24	Key IN	Key scan input.
25	GND	To be grounded.
27	Meter L-ch	A/D Convertor input for level meter indication.
28	Meter-R-ch	A/D Convertor input for level meter indication.
29	AVDD	+5V Power supply terminal of this IC.
30	AVref	Reference voltage input terminal.
31	GND	To be grounded.
32	XT2	Open
33	GND	To be grounded.
34	X1	Crystal element connecting terminal.
35	X2	
36	Key Mute	Rec mute control Mode (H = ON)
37	$\overline{\text{REC}}$	$\overline{\text{REC}}$ control Mode (L = ON)
38	LINE MUTE	Line mute control Mode (H = ON)
40	Dolby $\overline{\text{C}}$	Dolby $\overline{\text{C}}$ control Mode (L = ON)
41	Dolby $\overline{\text{B}}$	Dolby $\overline{\text{B}}$ control Mode (L = ON)
42	$\overline{\text{LINE}}$ / PB	$\overline{\text{LINE}}$ / PB control Mode
43	POWER	Power control Mode (H = ON)
44	GND	To be grounded.
45	T.P.S	T.P.S data input.
46	Hall	Hall IC data input.
47	Remocon IN	Remocon data input.
48	GND	To be grounded.
49	Remocon OUT	Remocon data output.
50	Close Motor	Close loadind Motor control (H = ON)
51	Open Motor	Open loading Motor control (H = ON)
52	VDD	+5V power supply terminal of this IC.
53	Close SW	Loading close detector sw input (L = ON).
54	Open SW	Loading open detector sw input (L = ON).
55	Rec (R) SW	Rec (Reverse) SW detector input.
56	Mode SW	Mode sw detector input.
57	TAPE SW	TAPE sw detector input.
58	Motor	Motor control output (H = ON)
59	Solenoid	Solenoid control output (H = ON)
60	Rec (F) SW	Rec (forward) sw detector input.
61~70	SEG1~SEG10	FIP segment control output.
71	V Load	(-24V) Negitive power supply input terminal for FIP blanking.
72~77	SEG11~SEG16	FIP segment control output.

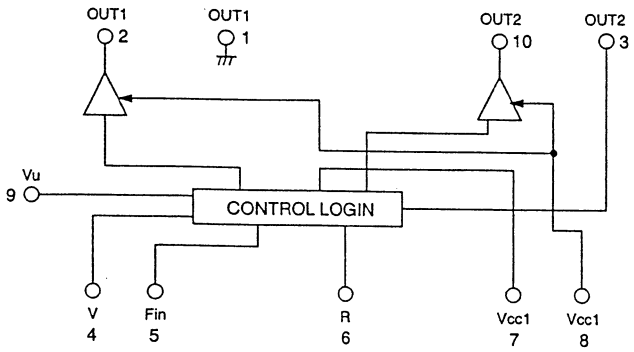
M5220P (DUAL LOW-Noise Operational Amplifiers) (DUAL POWER SUPPLY TYPE)



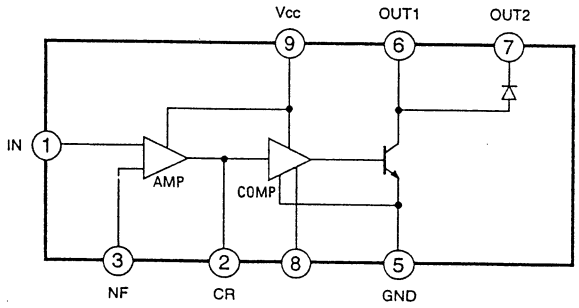
HA12142NT (DOLBY B. C Noise Reduction System)



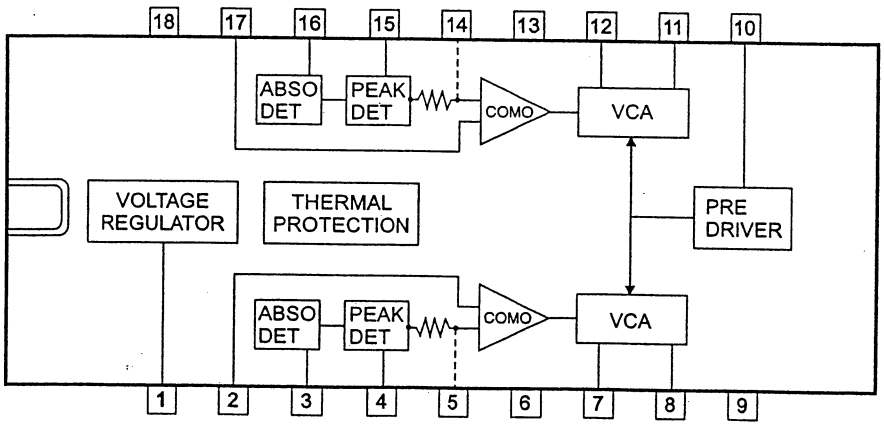
BA6209 (Reversible Motor Driver)



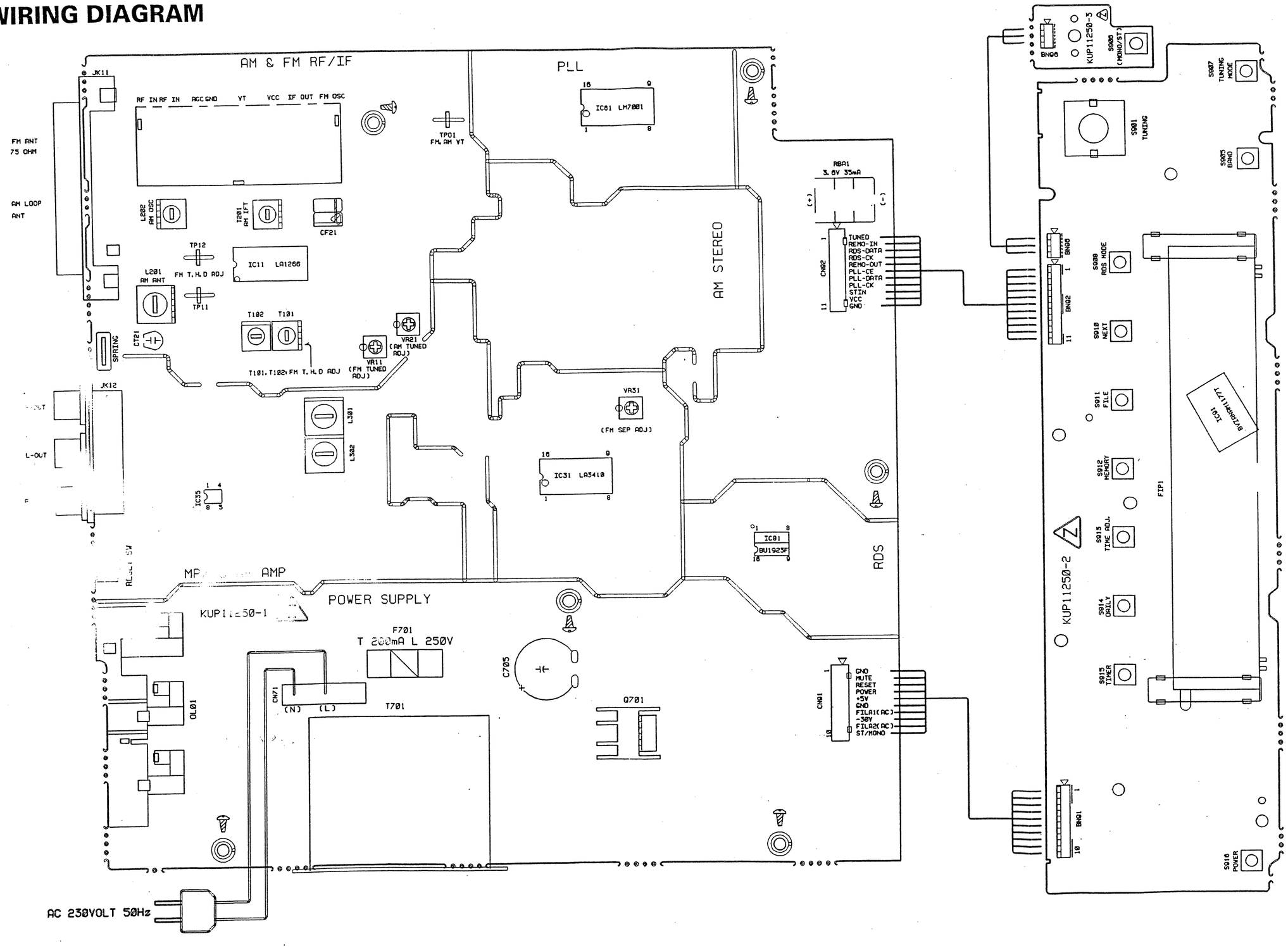
LA2000 (Audio Level Sensor)



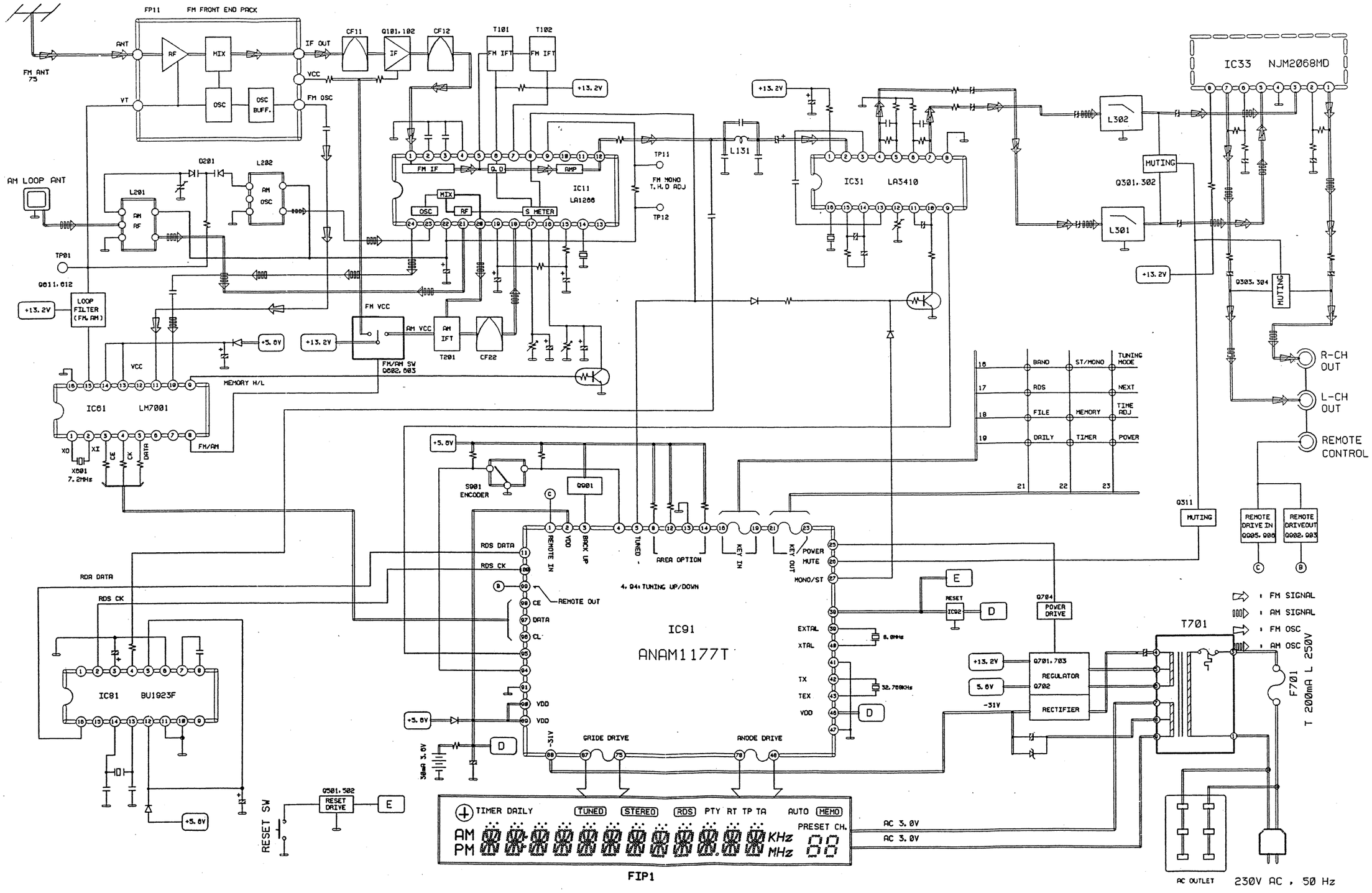
PC1297 (DOLBY HX PRO SYSTEM)



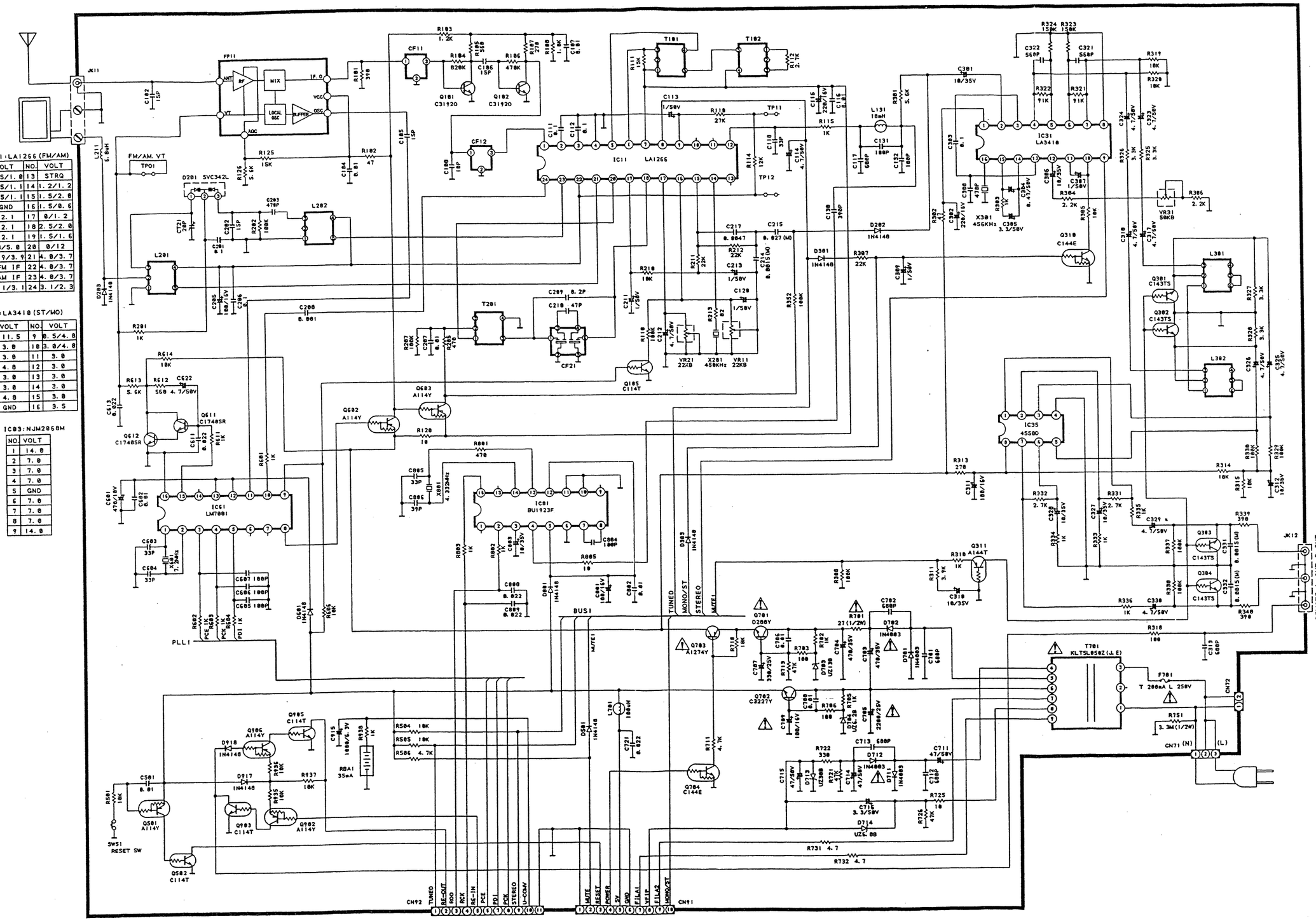
WIRING DIAGRAM



BLOCK DIAGRAM



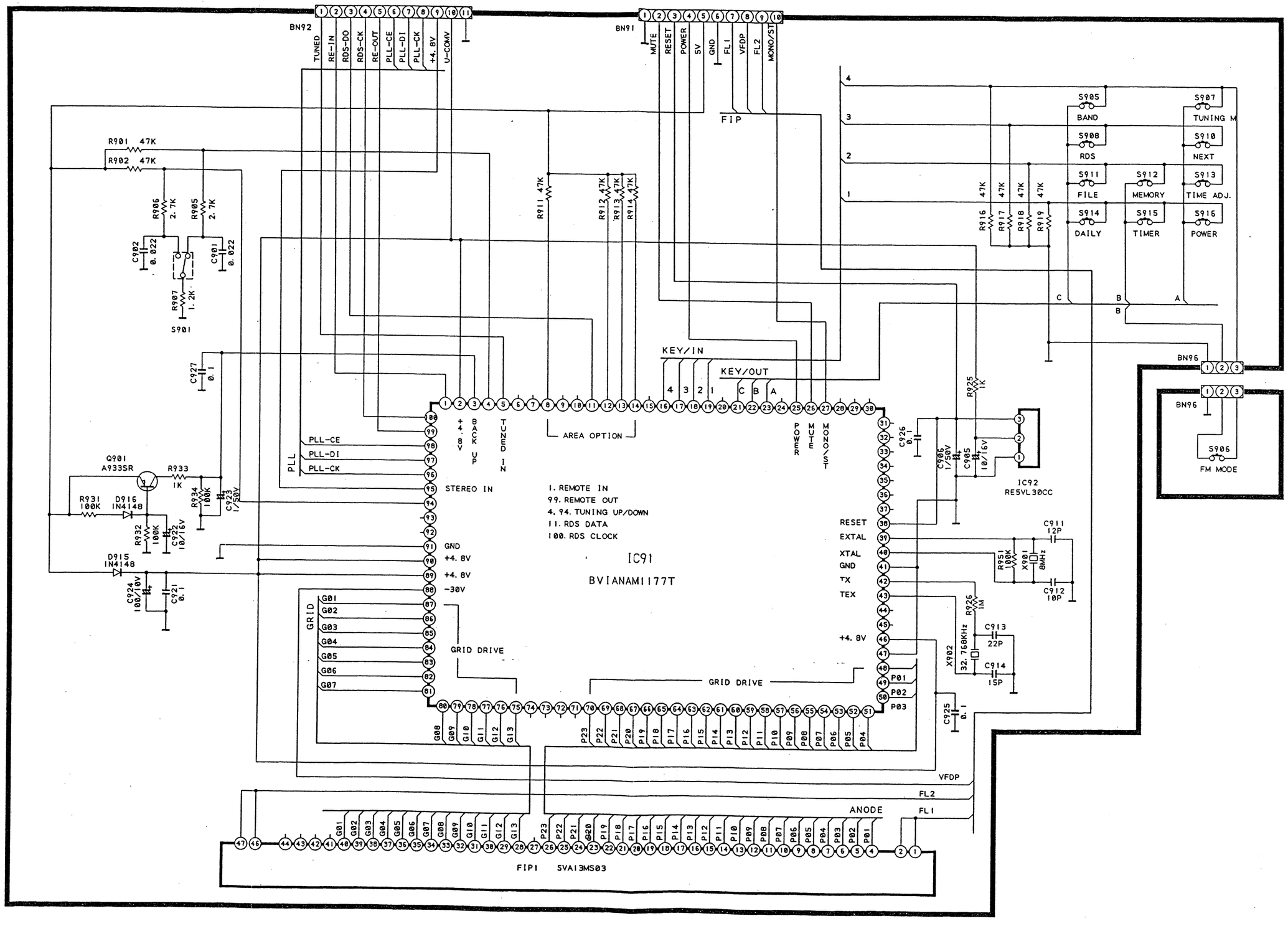
SCHEMATIC DIAGRAM



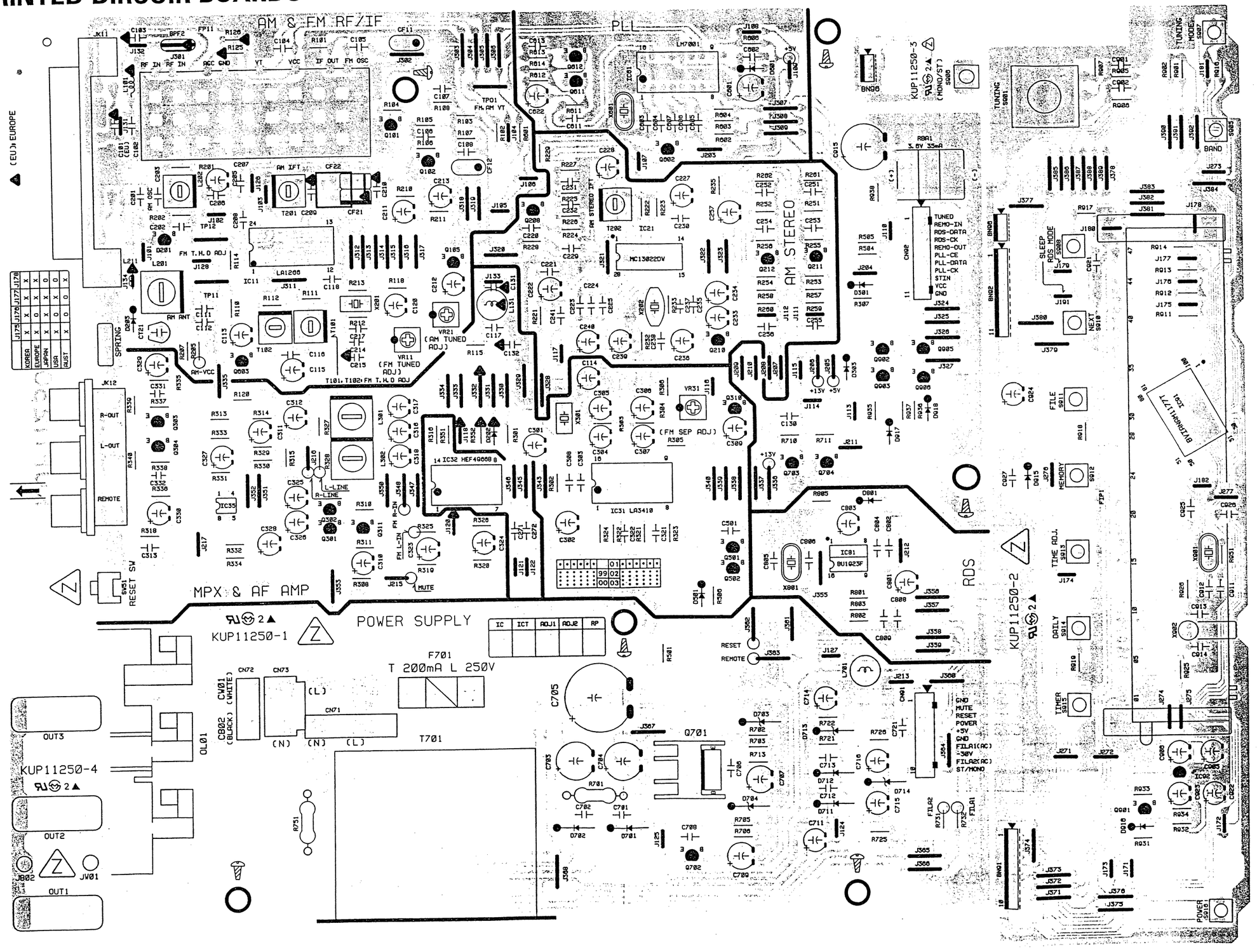
NO.	VOLT	NO.	VOLT
1	2.5/1.0	13	STRQ
2	2.5/1.1	14	1.2/1.2
3	2.5/1.1	15	1.5/2.0
4	GND	16	1.5/0.6
5	12.1	17	0/1.2
6	12.1	18	2.5/2.0
7	12.1	19	1.5/1.6
8	8/5.0	20	0/12
9	3.9/3.9	21	4.0/3.7
10	FM IF	22	4.0/3.7
11	AM IF	23	4.0/3.7
12	3.1/3.1	24	3.1/2.3

NO.	VOLT	NO.	VOLT
1	11.5	9	0.5/4.8
2	3.0	10	3.0/4.8
3	3.0	11	3.0
4	4.8	12	3.0
5	3.0	13	3.0
6	3.0	14	3.0
7	4.8	15	3.0
8	GND	16	3.5

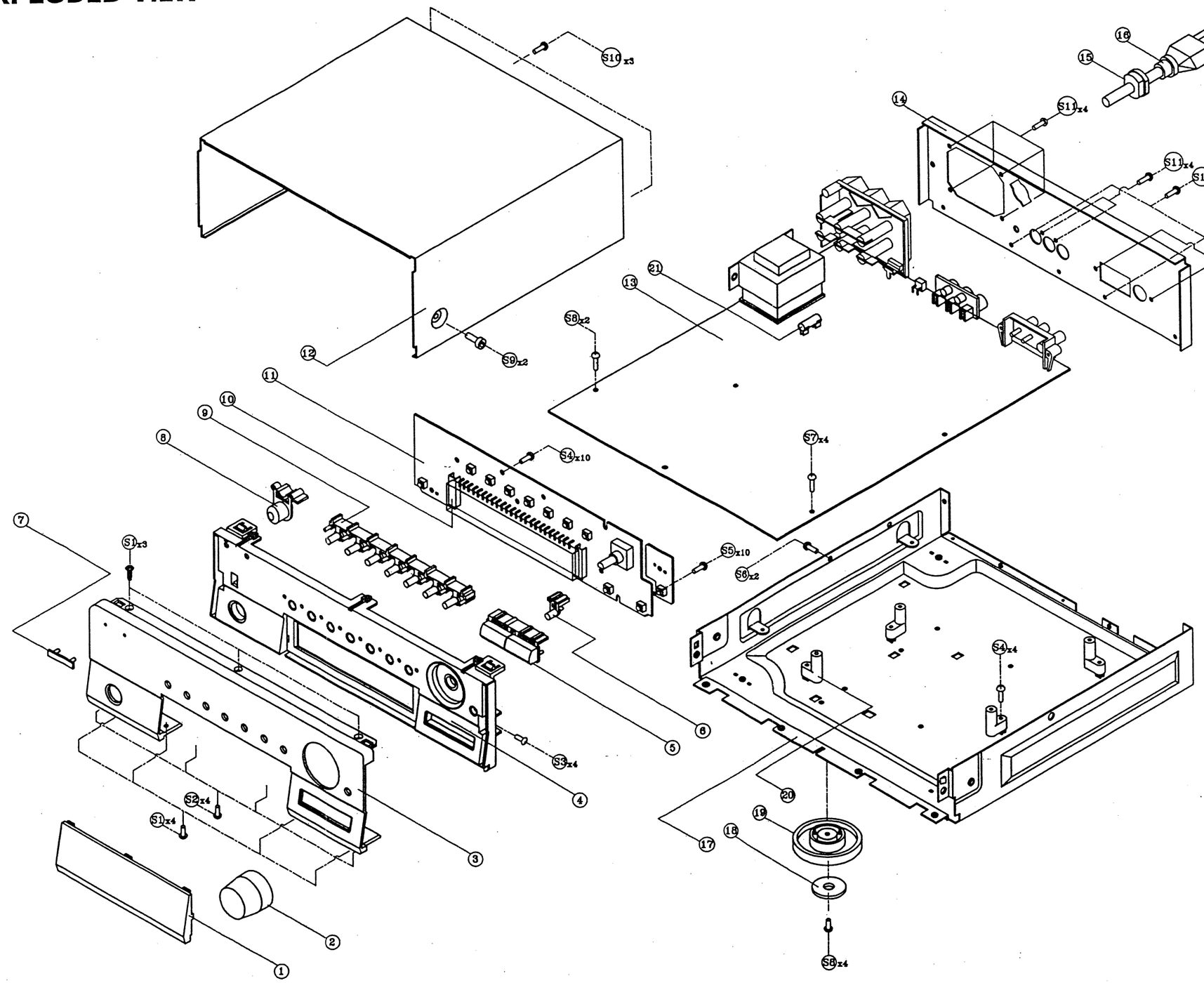
NO.	VOLT
1	14.0
2	7.0
3	7.0
4	7.0
5	GND
6	7.0
7	7.0
8	7.0
9	14.0


BN92
TUNED
RE-IN
RDS-DO
RDS-CK
RE-OUT
PLL-CE
PLL-DI
PLL-CK
+4.8V
U-COMV
BN91
MUTE
RESET
POWER
5V
GND
FL1
VFDP
FL2
MONO/ST
FIP
R901 47K
R902 47K
R906 2.7K
R905 2.7K
C902 0.022
C901 0.022
R907 1.2K
S901
R911 47K
R912 47K
R913 47K
R914 47K
S905 BAND
S907 TUNING M
S908 RDS
S910 NEXT
S911 FILE
S912 MEMORY
S913 TIME ADJ.
S914 DAILY
S915 TIMER
S916 POWER
R916 47K
R917 47K
R918 47K
R919 47K
KEY/IN
KEY/OUT
BN96
S906
FM MODE
C927 0.1
R925 1K
C926 0.1
C905 1/50V
C906 10/16V
IC92
RE5VL30CC
Q901
A933SR
R933 1K
R931 100K
D916 IN4148
R934 100K
C923 1/50V
R932 100K
C922 10/16V
D915 IN4148
C924 100/10V
C921 0.1
PLL
PLL-CE
PLL-DI
PLL-CK
STEREO IN
GND
+4.8V
+4.8V
-30V
+4.8V BACK UP
TUNED IN
AREA OPTION
PWM
MUTE
MONO/ST
1. REMOTE IN
99. REMOTE OUT
4. 94. TUNING UP/DOWN
11. RDS DATA
100. RDS CLOCK
IC91
BV1ANAM1177T
GRID
G01
G02
G03
G04
G05
G06
G07
G08
G09
G10
G11
G12
G13
GRID DRIVE
GRID DRIVE
P23
P22
P21
P20
P19
P18
P17
P16
P15
P14
P13
P12
P11
P10
P09
P08
P07
P06
P05
P04
P01
P02
P03
RESET
EXTAL
XTAL
GND
TX
TEX
+4.8V
C911 12P
R951 100K
X901 8MHz
C912 10P
R926 1M
C913 22P
X902 32.768KHz
C914 15P
C925 0.1
VFDP
FL2
FL1
ANODE
FIP1 SVA13MS03

PRINTED DIRCUIR BOARDS



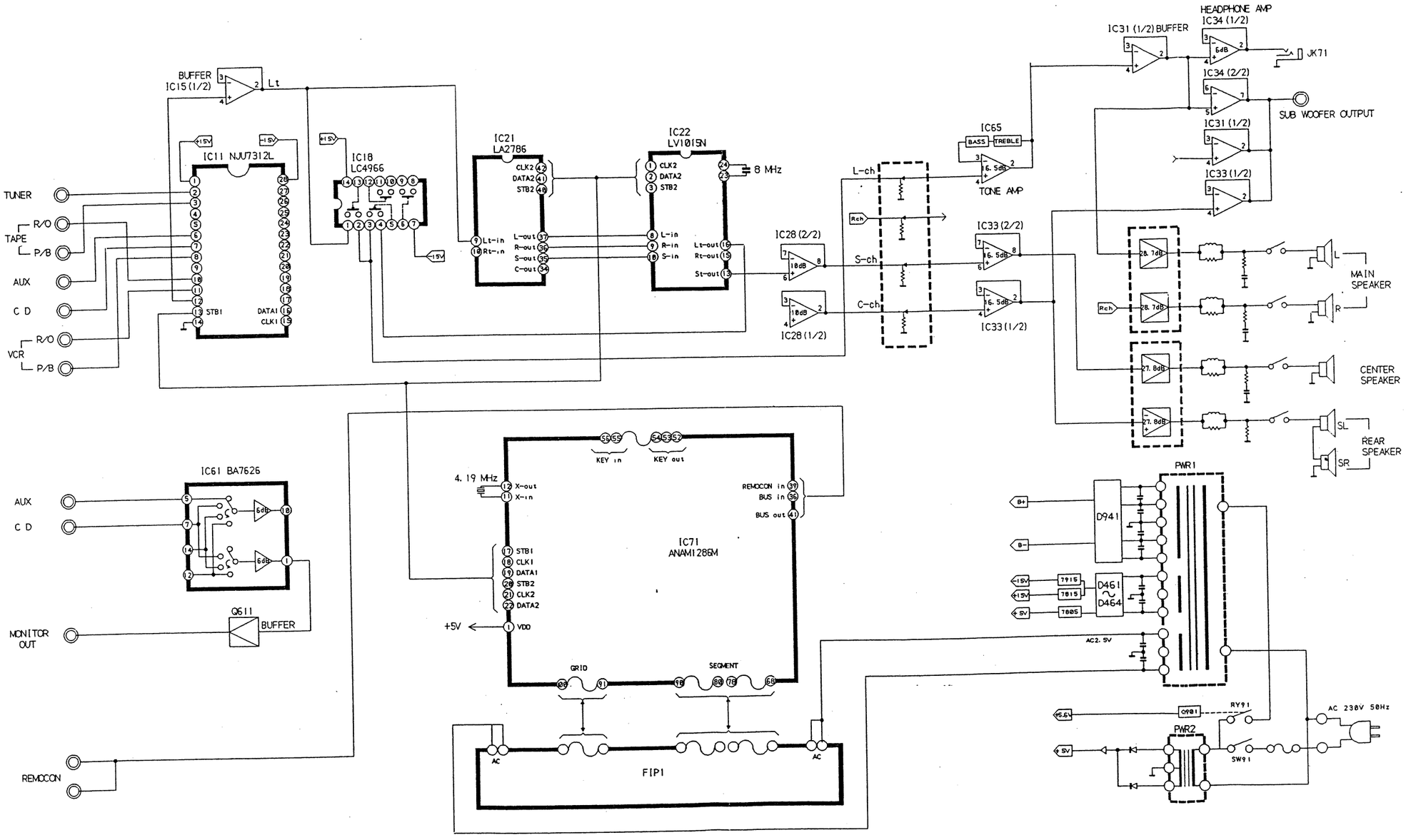
EXPLODED VIEW



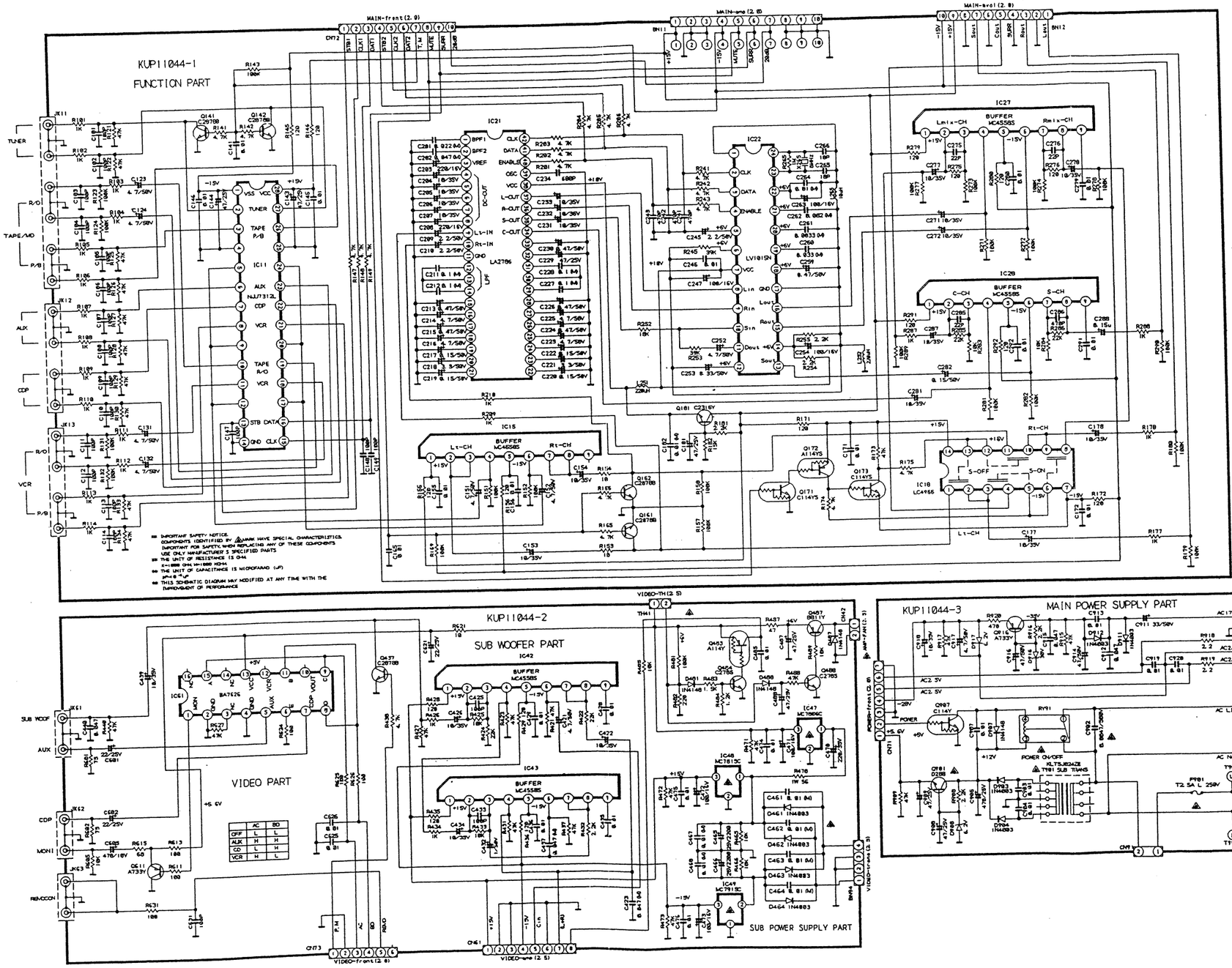
NO	PARTS - NO	DESCRIPSION	Q'Ty	REMARKS
1	KGU1A214A5X	WINDOW , FIP	1	
2	KGX1A275ZA	VOLUME CAP ASS'Y	1	
3	KKM1A089ZC19	PANEL , FRONT(AL)	1	
4	KGW1A259M7K78	PANEL , SUB(MOLD)	1	
5	KBT1A645M7K78	KNOB , TUNING	1	
6	KBT1A649M7K78	KNOB , STOP	1	
7	KGB1A082	BADGE	1	
8	KBT1A647M7K78	KNOB , POWER	1	
9	KBT3A390M7K79	KNOB , TACT (ST)	1	
10	KMD1A209	BRACKET , FIP	2	
11	KUP11250Z	SUB PCB ASS'Y	1	
12	KKC1B076S29	CABINET , TOP	1	
13	KUP11250Z	MAIN PCB ASS'Y	1	
14	KKF1A188Z	PANEL , REAR	1	
15	KHR129	BUSHING , AC CORD	1	
16	KJA2B019Z	AC CORD	1	
17	KUA1A134	CHASSIS , BOTTOM	1	
18	KHG1A039Z	CUSHION , FOOT	4	
19	KKL1A047M7H8	FOOT	4	
20	KHE1A027	SUPPORT , PCB	4	
21	KBA2C0200TLE	FUSE	1	
22				
23				
24				
25				
26				
27				
28				
29				
30				
31				
32				
33				

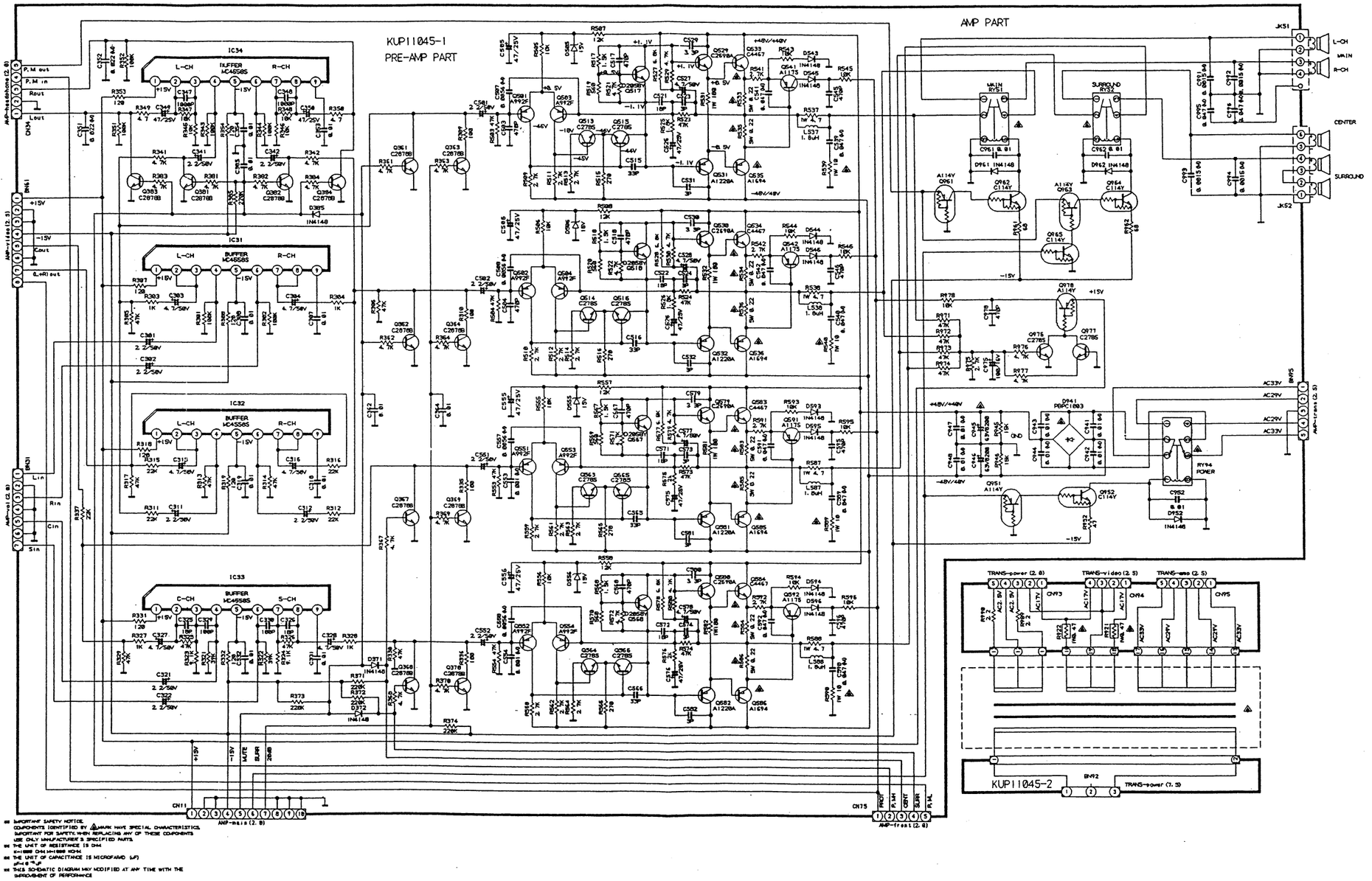
S1	KTS3+8G	SCREW	7	
S2	KTS3+8J	SCREW	4	
S3	KTB3+6J	SCREW	2	
S4	KTB3+10G	SCREW	14	
S5	STW3+10G	SCREW	1	
S6	KTB4+6FFZ	SCREW	2	
S7	KTB3+12G	SCREW	4	
S8	KTW3+8J	SCREW	6	
S9	KHD1A024FC	SCREW	2	
S10	KTB3+8JFC	SCREW	3	
S11	KTB3+10GFZ	SCREW	6	
S12	KTB3+8JFZ	SCREW	2	

BLOCK DIAGRAM

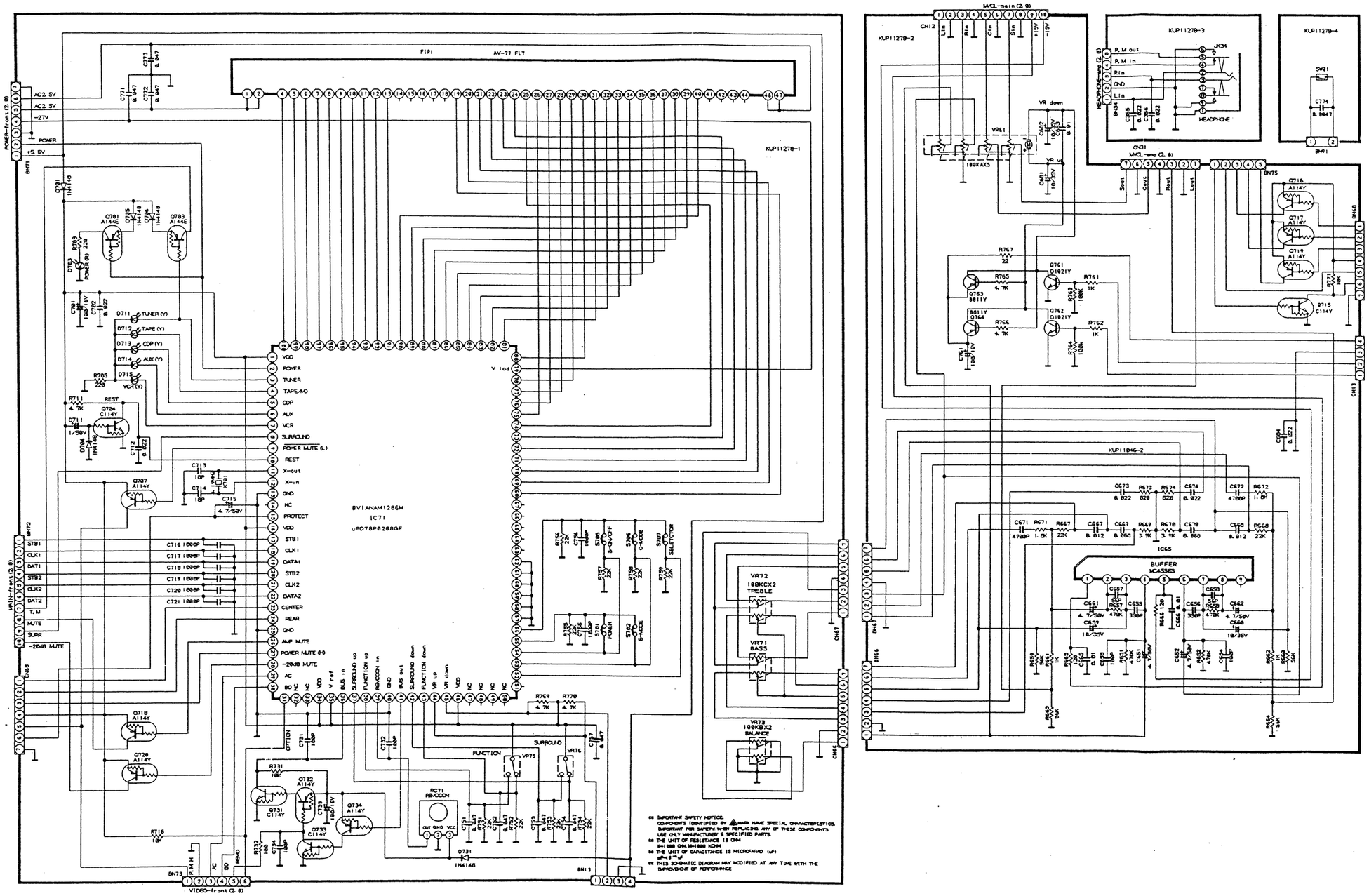


SCHEMATIC DIAGRAM





※ IMPORTANT SAFETY NOTICE
COMPONENTS IDENTIFIED BY ⚠ MARK HAVE SPECIAL CHARACTERISTICS.
IMPORTANT FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS
USE ONLY MANUFACTURER'S SPECIFIED PARTS.
※ THE UNIT OF RESISTANCE IS OHM
K=1000 OHM M=1000 KOHM
※ THE UNIT OF CAPACITANCE IS MICROFARD (uF)
uF=0.000001F
※ THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WITH THE
IMPROVEMENT OF PERFORMANCE


FIPI
AV-77 FLT
KUP11278-1
KUP11278-2
KUP11278-3
KUP11278-4
KUP11046-2
BVIANAM1286M
IC71
μPD78P8288GF
POWER-front (2, 8)
AC2.5V
AC2.5V
-27V
POWER
+5.6V
MAIN-front (2, 8)
VIDEO-front (2, 8)
HEADPHONE-amp (2, 8)
HEADPHONE
MAIN-main (2, 8)
MAIN-amp (2, 8)
BUFFER
VR down
VR72 100KCX2 TREBLE
VR71 BASS
VR73 100KBX2 BALANCE
VR75 FUNCTION
VR76 SURROUND
TUNER (Y)
TAPE (Y)
CDP (Y)
AUX (Y)
VCR (Y)
REST
POWER (R)
-20dB MUTE
POWER MUTE (L)
REMOCON
REMOCON in
OPTION
FUNCTION
SURROUND
S-ON/OFF
S-MODE
C-MODE
SELECTION
VDD
TUNER
TAPE/MD
CDP
AUX
VCR
SURROUND
REST
X-out
X-in
GND
NC
PROTECT
VDD
STB1
CLK1
DATA1
STB2
CLK2
DATA2
CENTER
REAR
GND
AMP MUTE
POWER MUTE (H)
-20dB MUTE
AC
BD
NC
VDD
V ref
BUS in
SURROUND up
FUNCTION up
REMOCON in
GND
BUS out
SURROUND down
FUNCTION down
VR up
VR down
VDD
NC
NC
NC
NC
V lod
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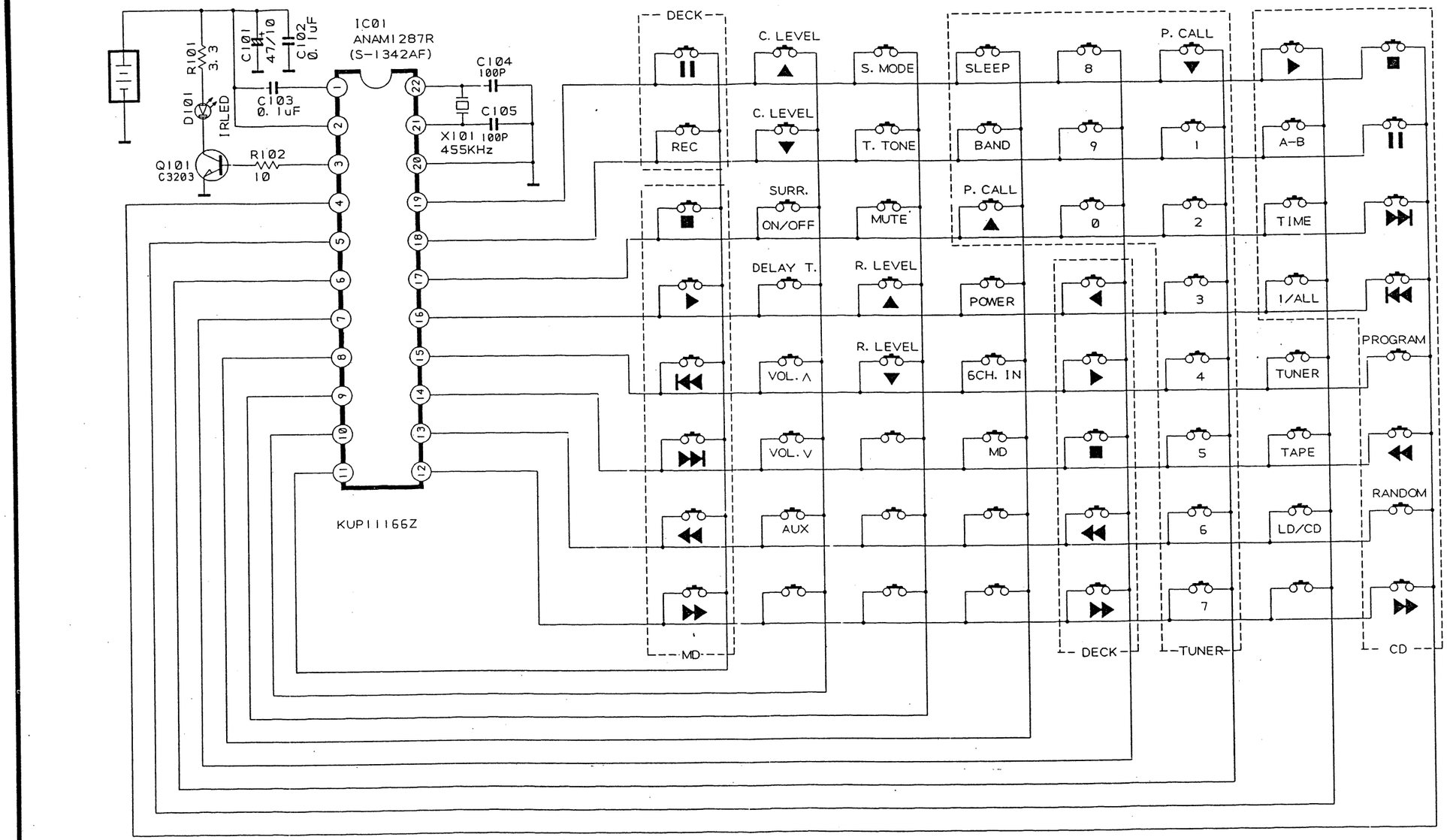
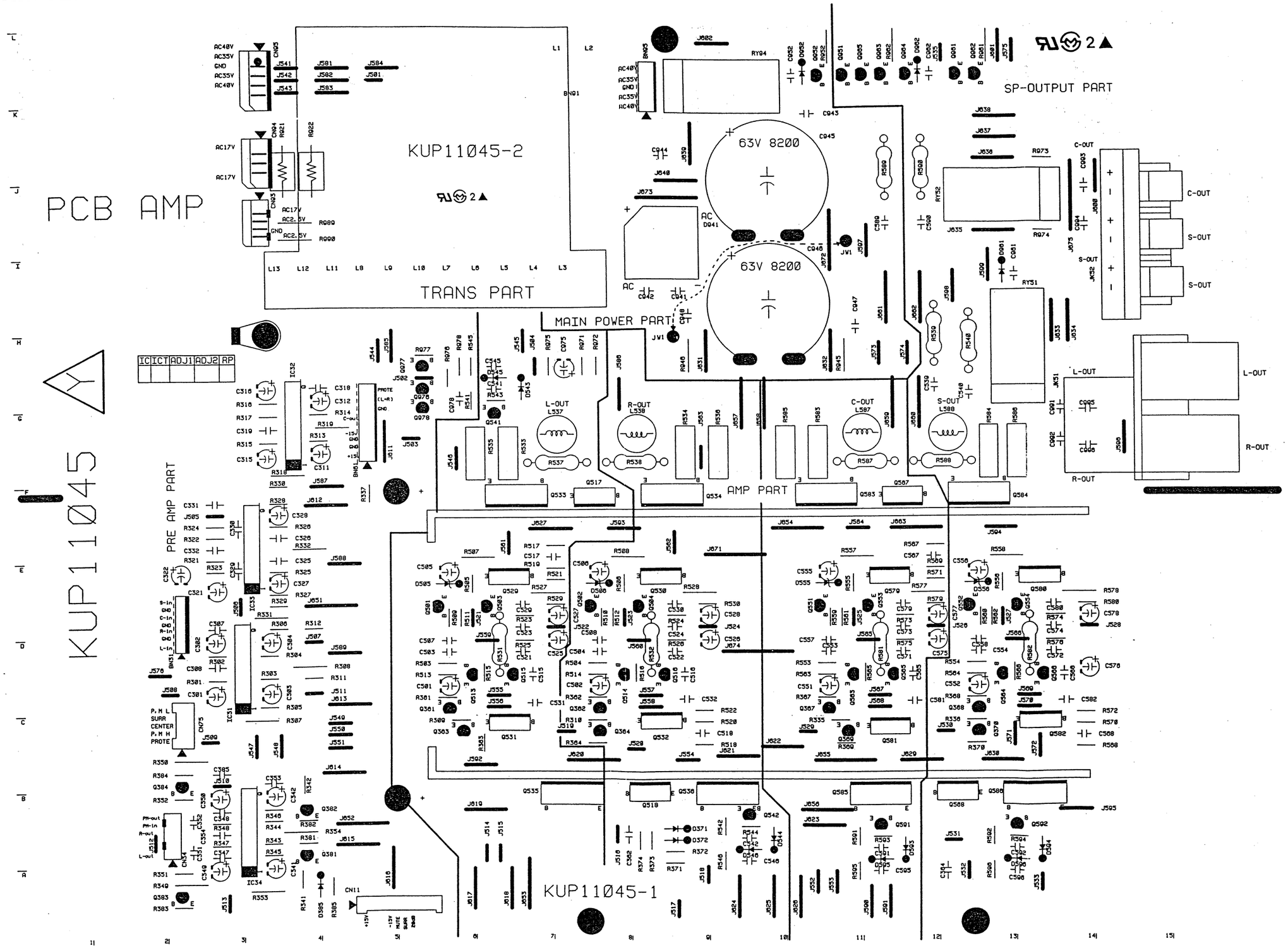
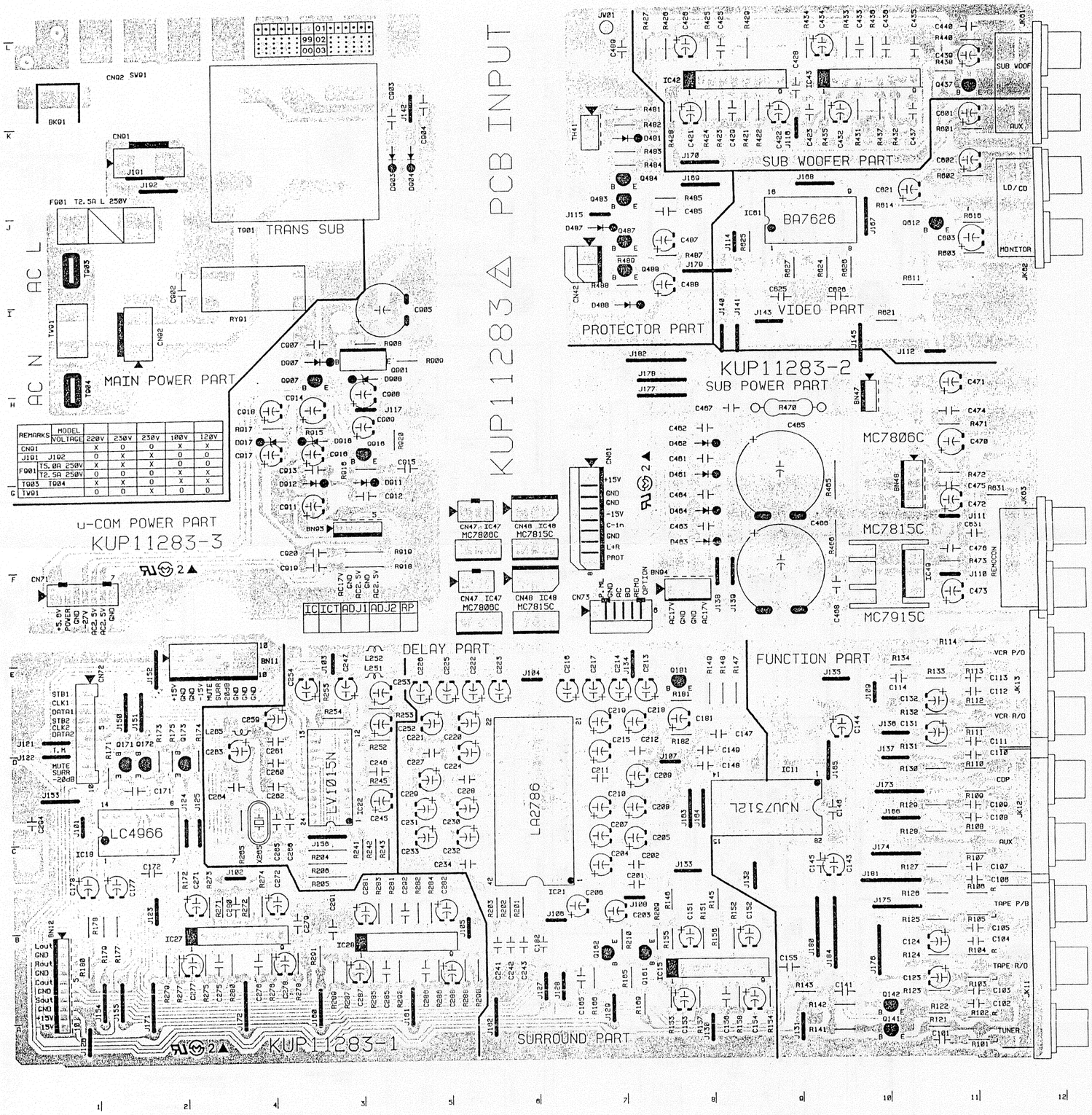
COMPONENTS IDENTIFIED BY ⚠ MARK HAVE SPECIAL CHARACTERISTICS IMPORTANT FOR SAFETY. WHEN REPLACING ANY OF THESE COMPONENTS USE ONLY MANUFACTURER'S SPECIFIED PARTS.
** THE UNIT OF RESISTANCE IS OHM
K=1000 OHM M=1000 KOHM
** THE UNIT OF CAPACITANCE IS MICROFARAD (μF)
P=10^-6 μF
** THIS SCHEMATIC DIAGRAM MAY MODIFIED AT ANY TIME WITH THE IMPROVEMENT OF PERFORMANCE


IC01
ANAM1287R
(S-1342AF)
KUP1166Z
R101 3.3
C101 47/10
C102 0.1UF
C103 0.1uF
D101 IRLED
Q101 C3203
R102 10
C104 100P
C105 100P
X101 455KHz
DECK
C. LEVEL
S. MODE
SLEEP
8
P. CALL
REC
C. LEVEL
T. TONE
BAND
9
1
A-B
SURR. ON/OFF
MUTE
P. CALL
0
2
TIME
DELAY T.
R. LEVEL
POWER
3
1/ALL
R. LEVEL
VOL. ∧
6CH. IN
4
TUNER
PROGRAM
VOL. V
MD
5
TAPE
RANDOM
AUX
6
LD/CD
7
MD
DECK
TUNER
CD

PRINTED DIRCUIR BOARDS



KUP11283△ PCB INPUT



REMARKS	MODEL VOLTAGE	220V	230V	210V	100V	120V
CN01		X	O	O	X	X
J101 J102		O	X	X	O	O
F001	T5.0A 250V	X	X	X	O	O
	T2.5A 250V	O	O	O	X	X
T003 T004		X	X	O	X	X
TV01		O	O	X	O	O

KUP11278Z FRONT PCB

DIPPING

KUP11278Z-3 HEADPHONE PCB

KUP11278Z-4 MOMS SW PCB

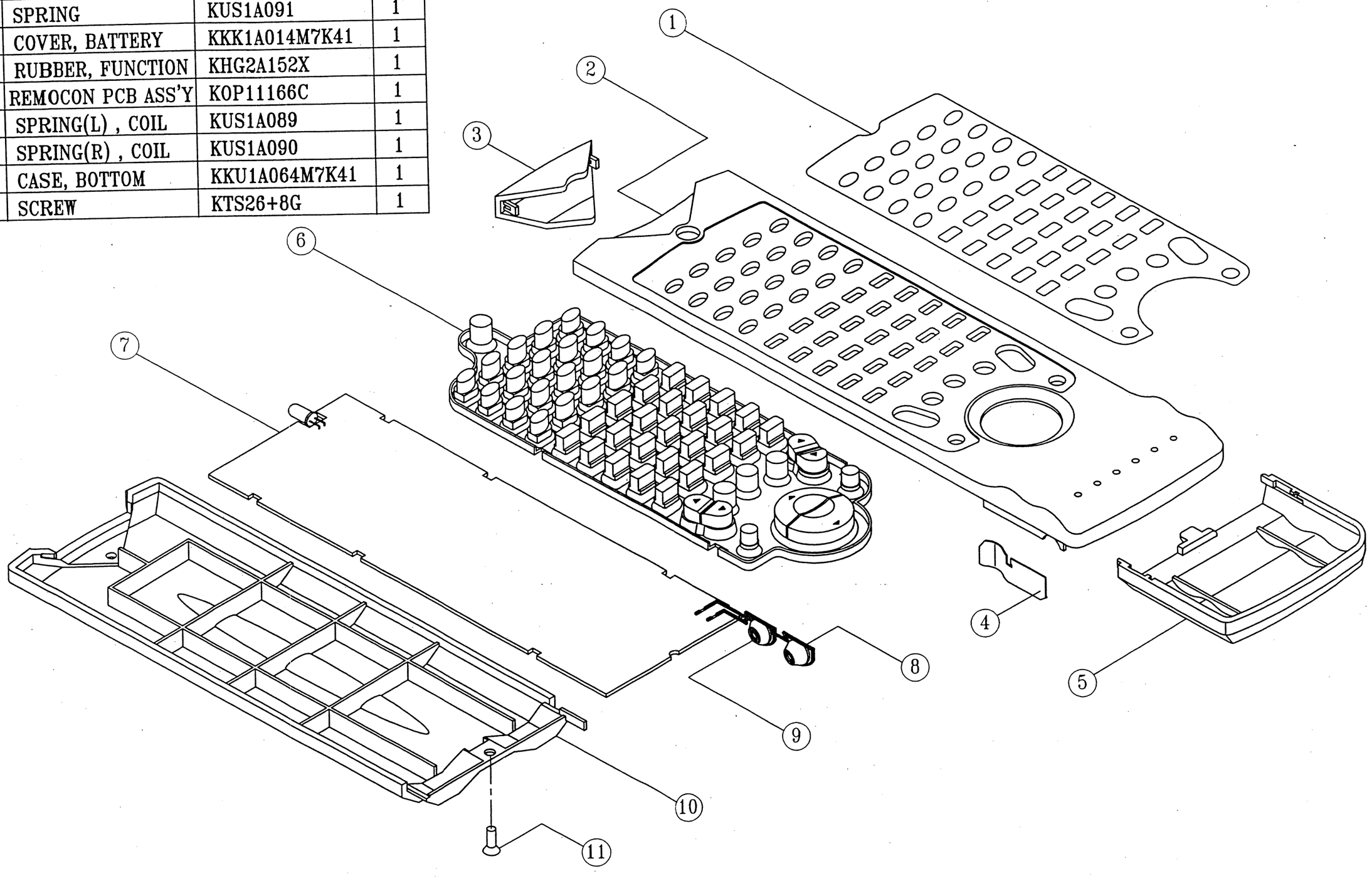
KUP11278Z-2 MOTOR VR TONE PCB

KUP11278Z-1 MICOM PCB

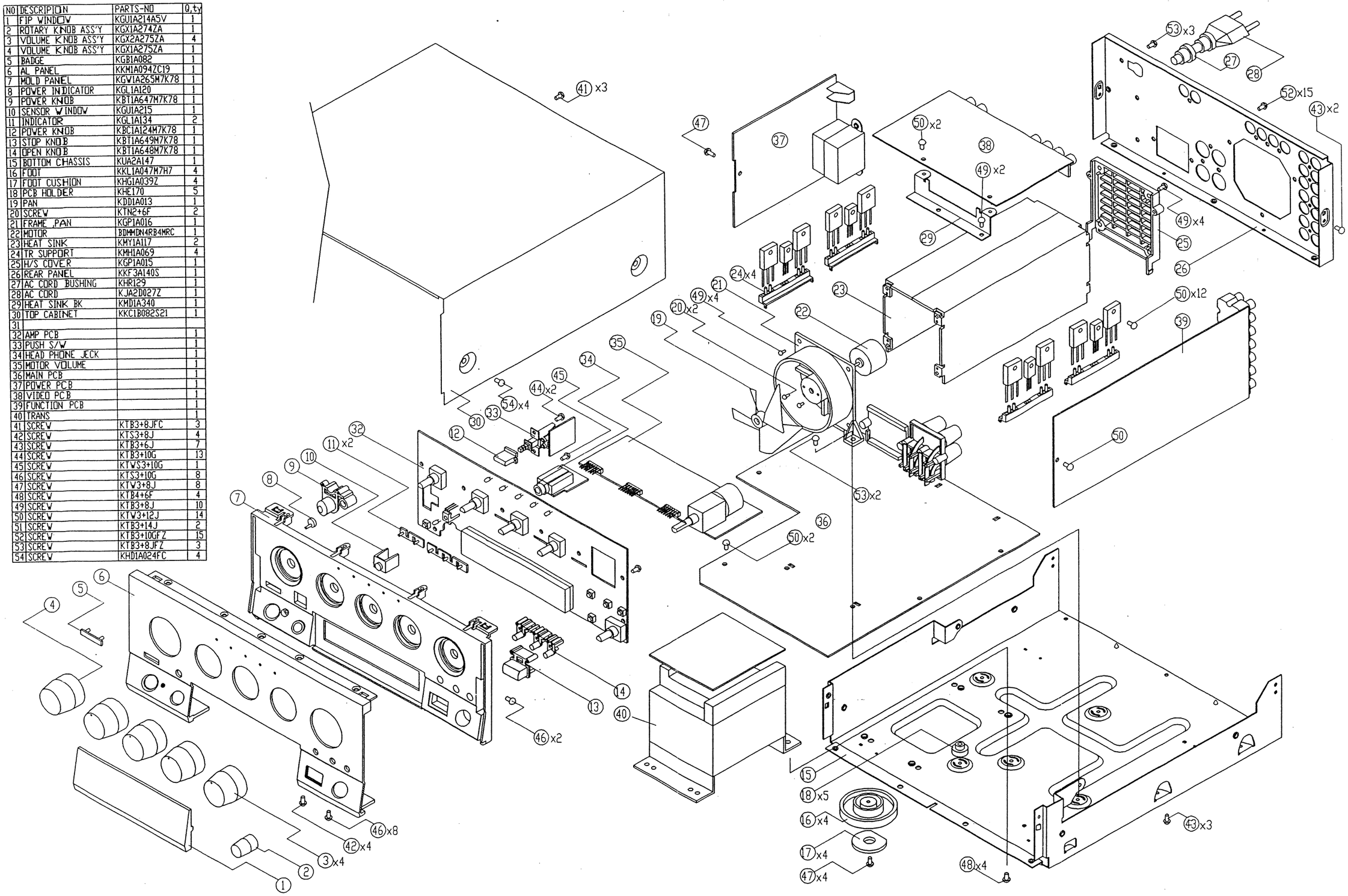
1 2 3 4 5 6 7 8

EXPLODED VIEW

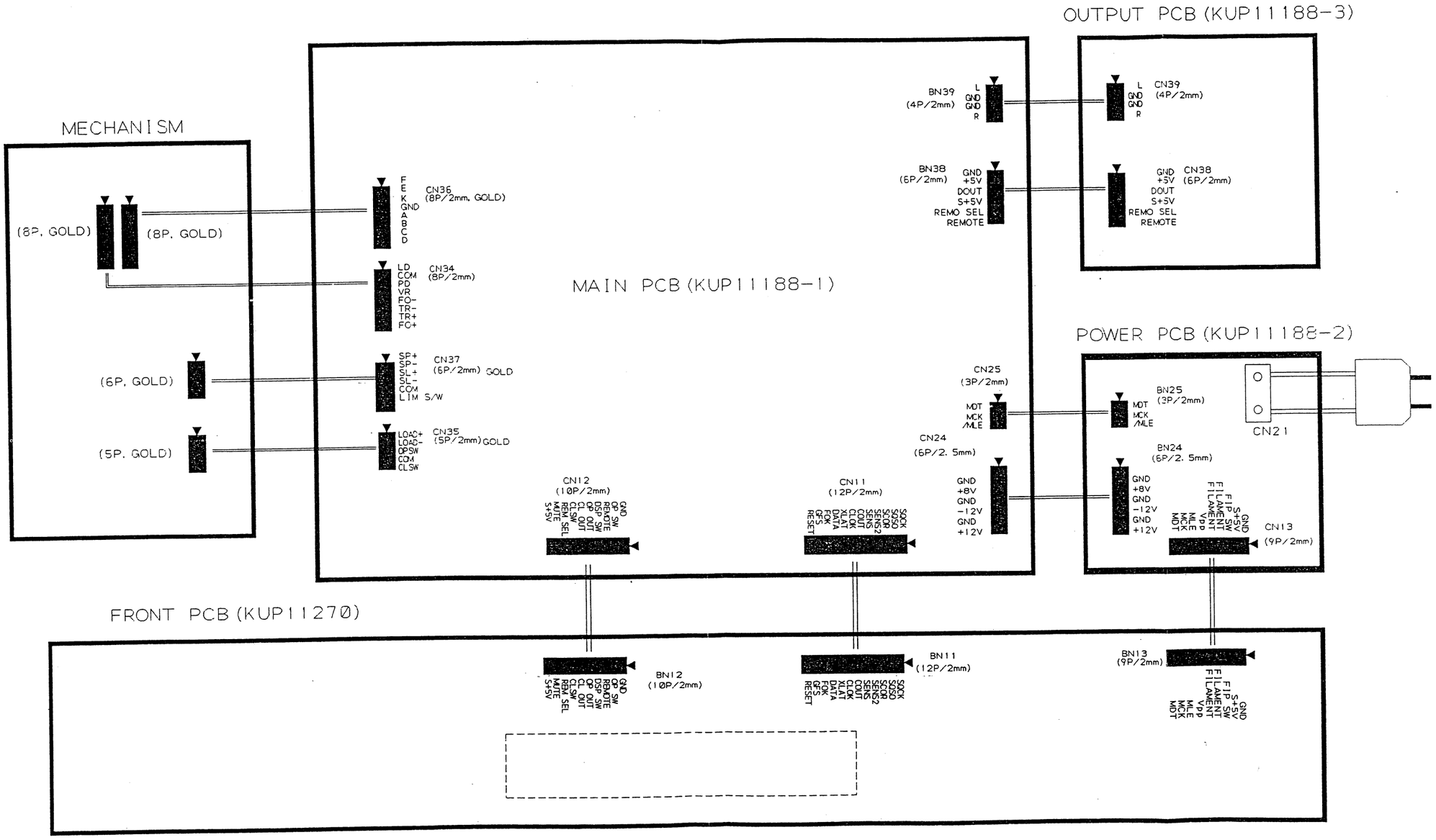
NO.	DESCRIPTION	PARTS-NO	Q'TY
1	SHEET, FUNCTION	KGX2A254X	1
2	CASE , TOP	KKM1A076M7XK41	1
3	WINDOW	KGU1A178	1
4	SPRING	KUS1A091	1
5	COVER, BATTERY	KKK1A014M7K41	1
6	RUBBER, FUNCTION	KHG2A152X	1
7	REMOCON PCB ASS'Y	KOP11166C	1
8	SPRING(L) , COIL	KUS1A089	1
9	SPRING(R) , COIL	KUS1A090	1
10	CASE, BOTTOM	KKU1A064M7K41	1
11	SCREW	KTS26+8G	1



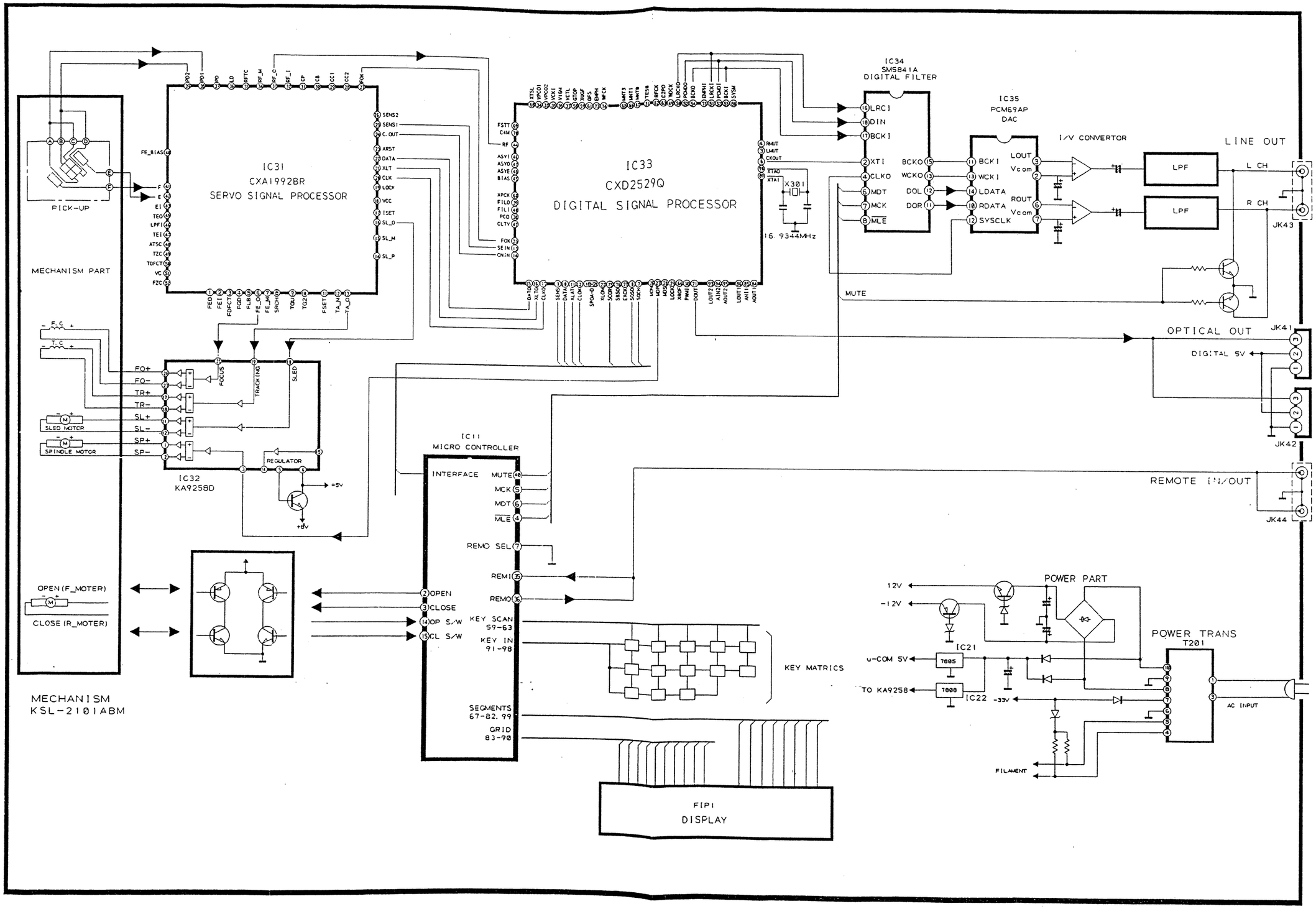
NO	DESCRIPTION	PARTS-NO	Q,ty
1	FIP WINDOW	KGU1A214A5V	1
2	ROTARY KNOB ASS'Y	KGX1A274ZA	1
3	VOLUME KNOB ASS'Y	KGX2A275ZA	4
4	VOLUME KNOB ASS'Y	KGX1A275ZA	1
5	BADGE	KGB1A082	1
6	AL PANEL	KKM1A094ZC19	1
7	MOLD PANEL	KGW1A265M7K78	1
8	POWER INDICATOR	KGL1A120	1
9	POWER KNOB	KBT1A647M7K78	1
10	SENSOR WINDOW	KGU1A215	1
11	INDICATOR	KGL1A134	2
12	POWER KNOB	KBC1A124M7K78	1
13	STOP KNOB	KBT1A649M7K78	1
14	OPEN KNOB	KBT1A648M7K78	1
15	BOTTOM CHASSIS	KUA2A147	1
16	FOOT	KKL1A047M7H7	4
17	FOOT CUSHION	KHG1A039Z	4
18	PCB HOLDER	KHE170	5
19	PAN	KDD1A013	1
20	SCREW	KTN2+6F	2
21	FRAME ,PAN	KGP1A016	1
22	MOTOR	BDMMDN4RB4MRC	1
23	HEAT SINK	KMY1A117	2
24	TR SUPPORT	KMH1A069	4
25	H/S COVER	KGP1A015	1
26	REAR PANEL	KKF3A140S	1
27	AC CORD BUSHING	KHR129	1
28	AC CORD	KJA2D027Z	1
29	HEAT SINK BK	KMD1A340	1
30	TOP CABINET	KKC1B082S21	1
31			
32	AMP PCB		1
33	PUSH S/W		1
34	HEAD PHONE JECK		1
35	MOTOR VOLUME		1
36	MAIN PCB		1
37	POWER PCB		1
38	VIDEO PCB		1
39	FUNCTION PCB		1
40	TRANS		1
41	SCREW	KTB3+8JFC	3
42	SCREW	KTS3+8J	4
43	SCREW	KTB3+6J	7
44	SCREW	KTB3+10G	13
45	SCREW	KTWS3+10G	1
46	SCREW	KTS3+10G	8
47	SCREW	KTW3+8J	8
48	SCREW	KTB4+6F	4
49	SCREW	KTB3+8J	10
50	SCREW	KTW3+12J	14
51	SCREW	KTB3+14J	2
52	SCREW	KTB3+10GFZ	15
53	SCREW	KTB3+8JFZ	3
54	SCREW	KHD1A024FC	4



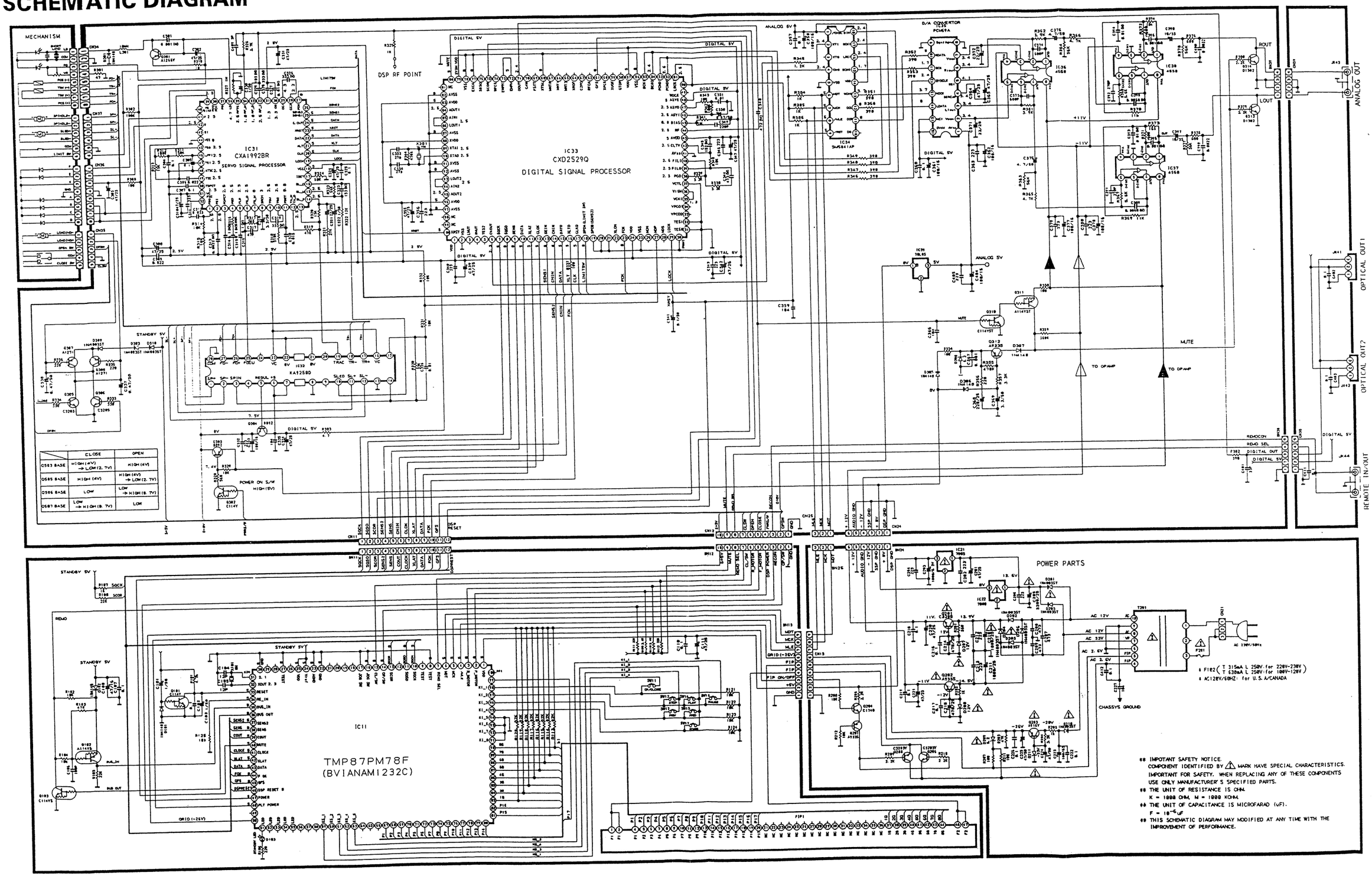
WIRING DIAGRAM



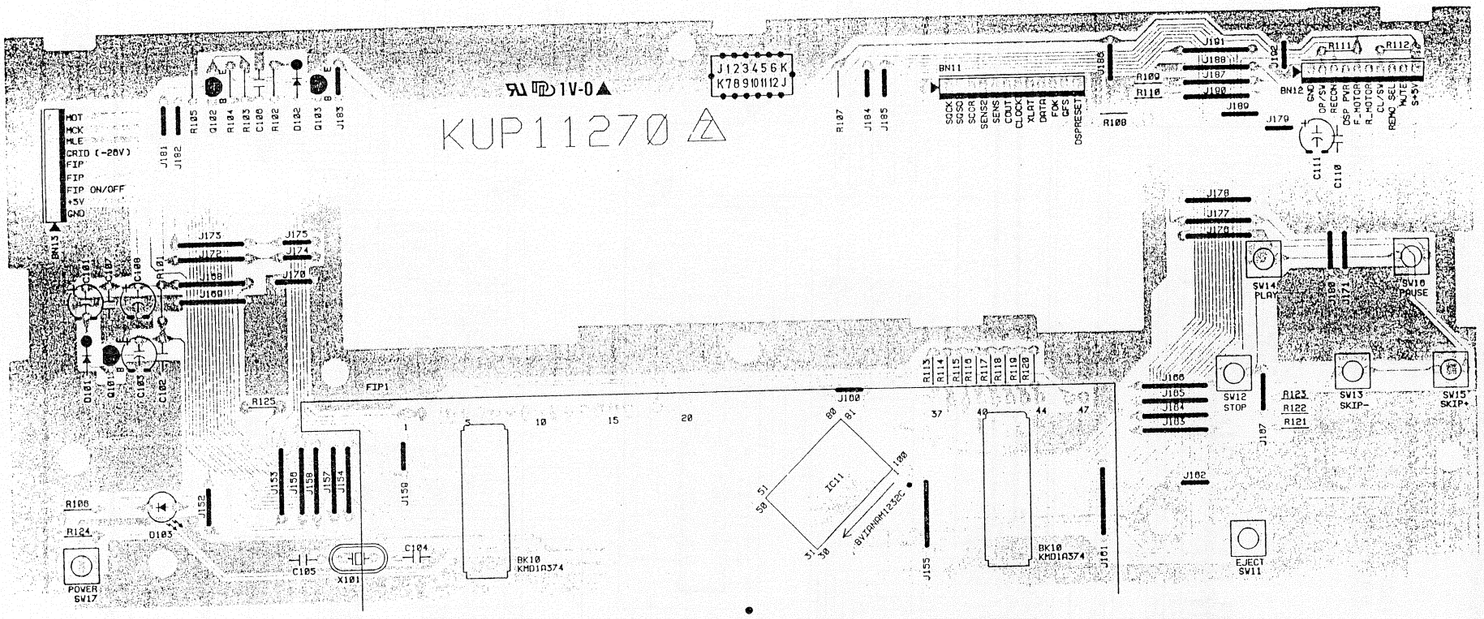
BLOCK DIAGRAM

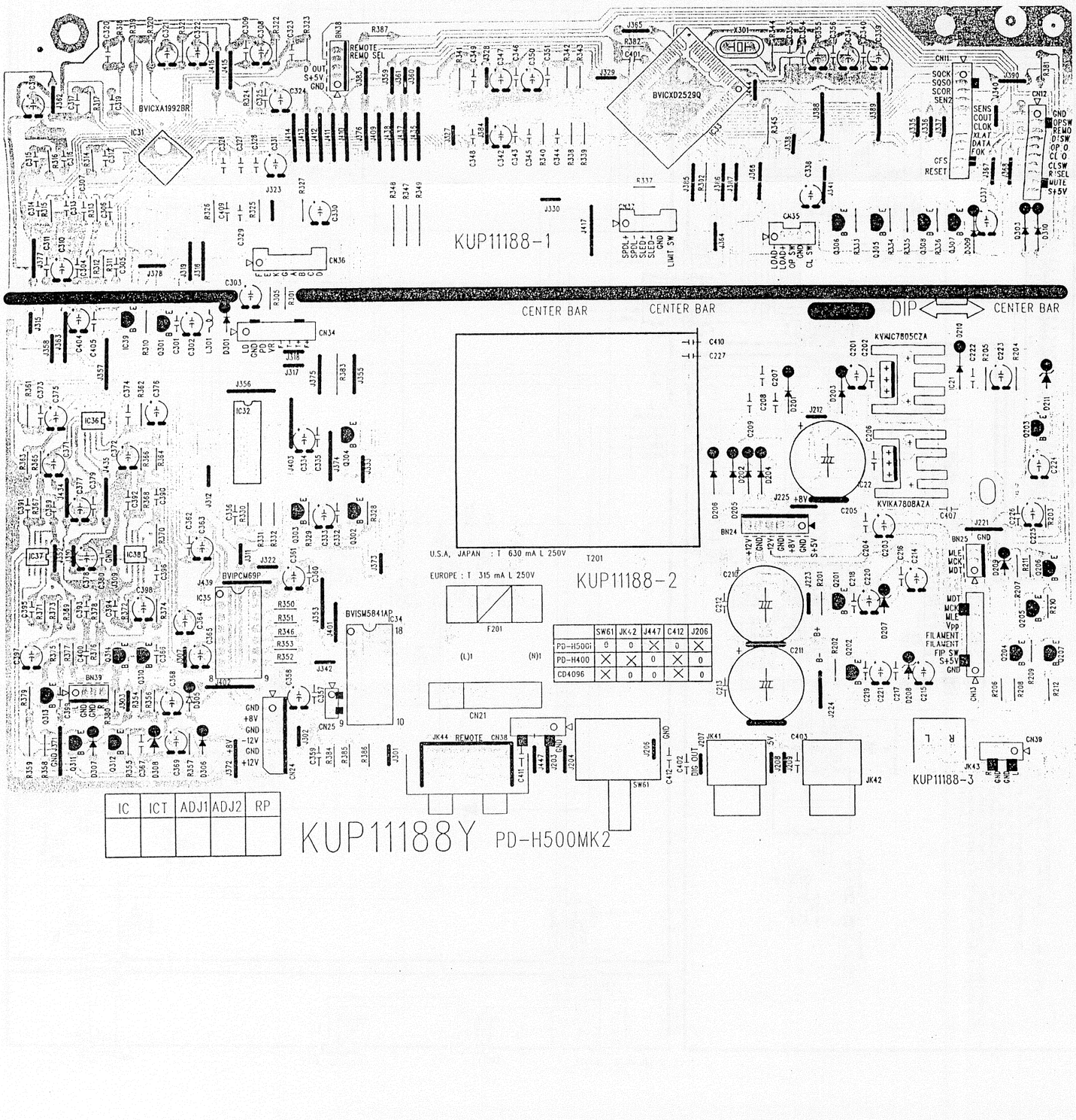


SCHEMATIC DIAGRAM



PRINTED DIRCUIR BOARDS



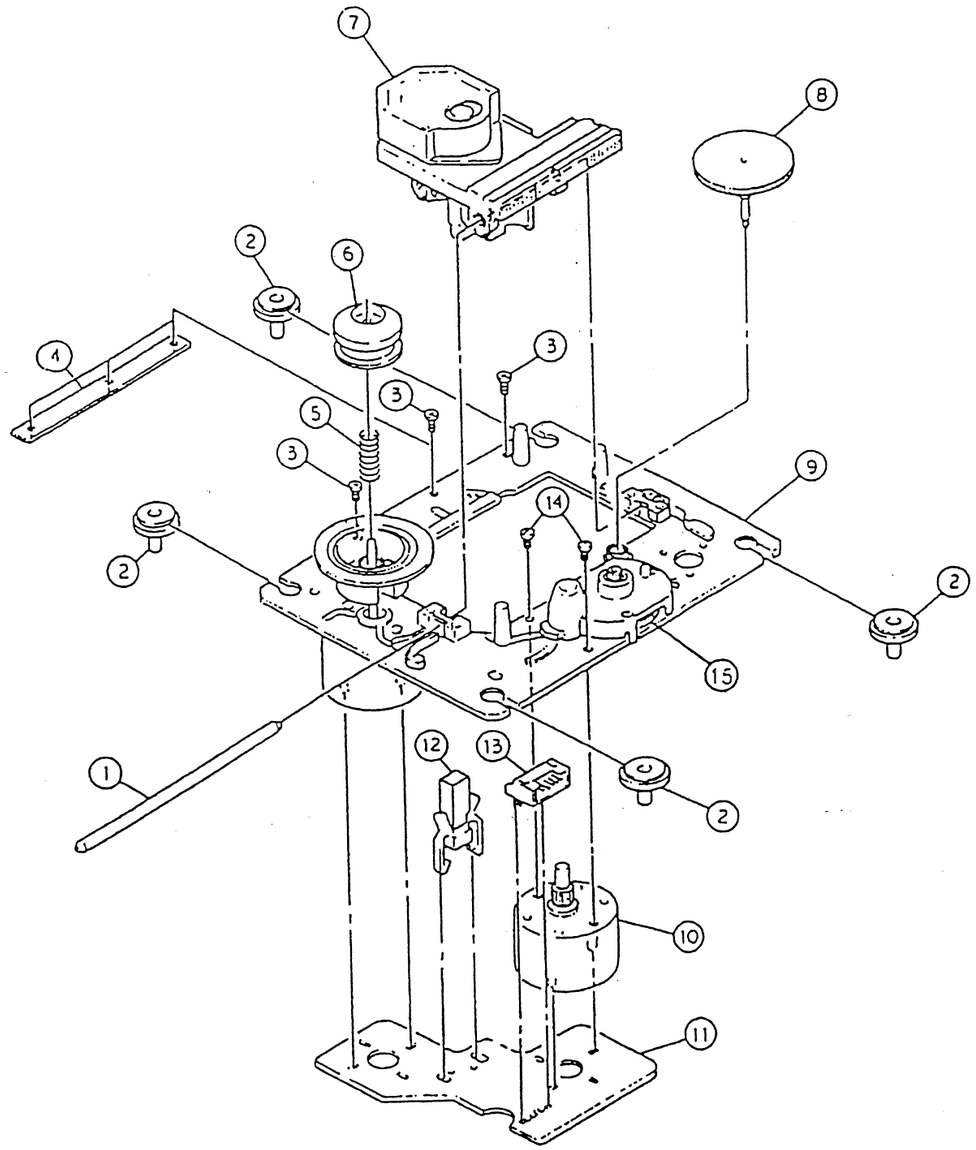


	SW61	JK42	J447	C412	J206
PD-H500i	0	0	X	0	X
PD-H400	X	X	0	X	0
CD4096	X	0	0	X	0

IC	ICT	ADJ1	ADJ2	RP

MECHANISM ASS'Y

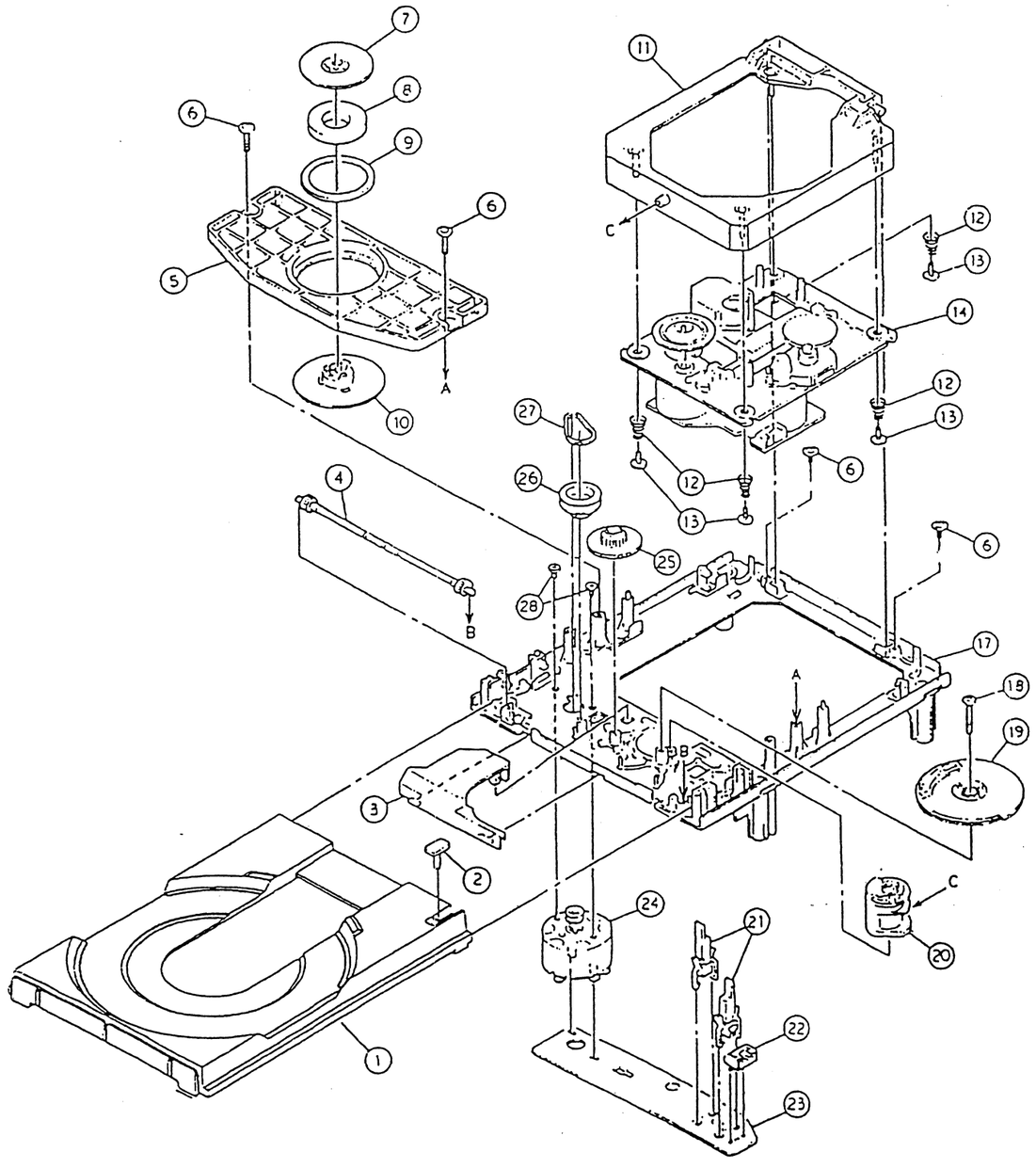
KSM-2101ABM
Disassembly Drawing



MECHANISM ASS'Y (KSM-2101ABM)

REF. NO.	PARTS NO.	DESCRIPTION	REMARKS
2- 1	2-626-908-01	SLED SHAFT (S)	
2- 2	2-625-538-01	INSULATOR (S)	
2- 3	2-641-386-01	SCREW (2X5), TAPPING (S)	
2- 4	2-625-625-01	REINFORCEMENT(S)	
2- 5	2-625-465-01	SPRING (S), COMPRESSION	
2- 6	2-625-477-01	RING (LO)(S),CENTER	
2- 7	8-848-127-31	PIKU UP	
2- 8	2-625-462-02	GEAR (A)(S)	
2- 9	X-2625-133-2	CHASSIS ASSY (MB), TT	
2-10	X-2625-132-1	GEAR ASSY (MB), MOTOR	
2-11	1-639-678-13	MOTOR PCB (6P)(S)	
2-12	1-572-085-12	SWITCH, LEAF	
2-13	1-564-722-11	PIN, CONNECTOR 6P	
2-14	7-621-255-15	SCREW +P2X3	
2-15	2-626-081-01	GEAR (B)	

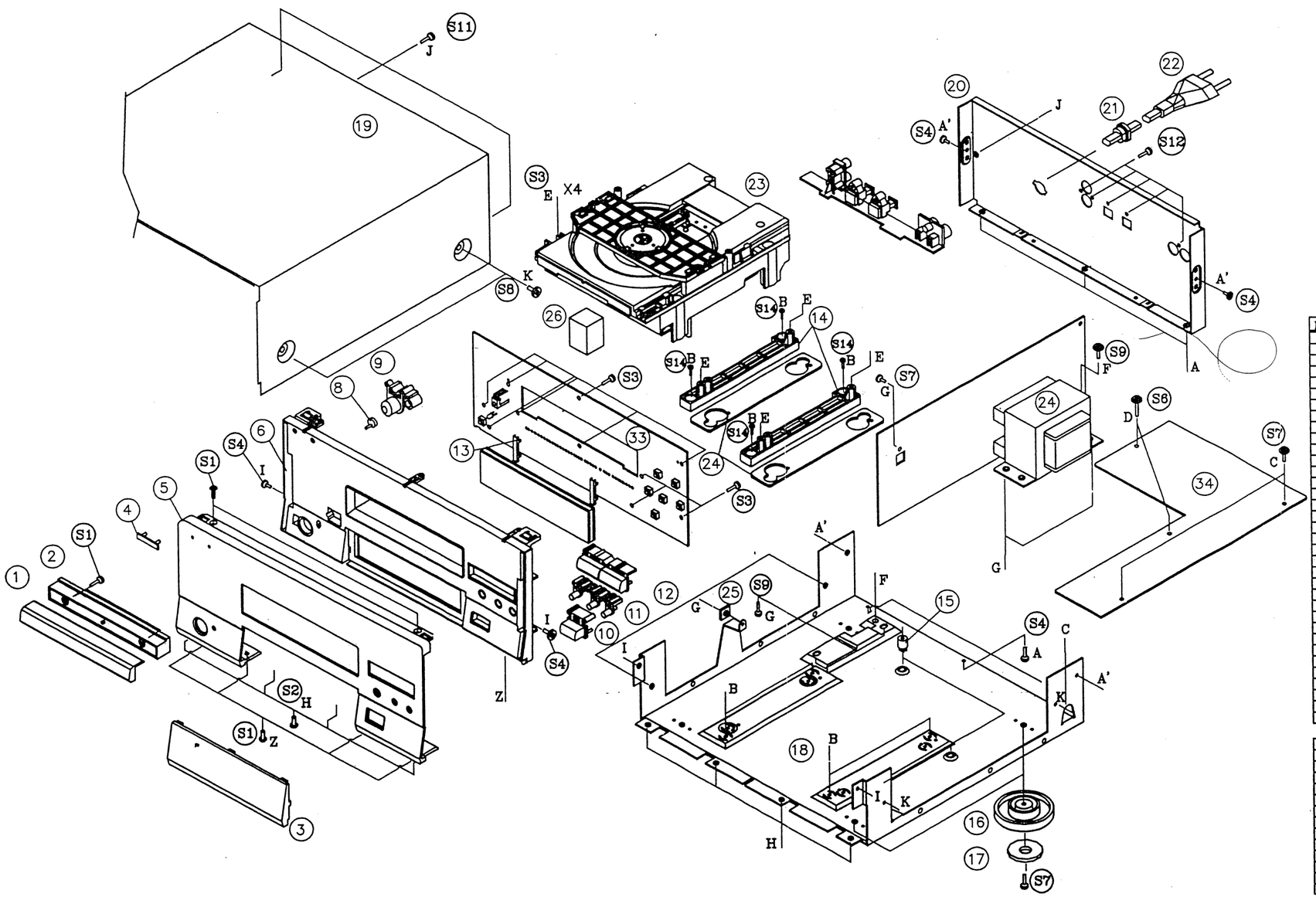
KSL-2101ABM
Disassembly Drawing



MECHANISM ASS'Y (KSM-2101ABM)

REF. NO.	PARTS NO.	DESCRIPTION	REMARKS
1- 1	2-625-550-03	TRAY (S)	
1- 2		VACANT	
1- 3	2-625-544-02	GEAR COVER (S)	
1- 4	2-625-535-01	TRAY GEAR	
1- 5	2-625-546-01	CHUCKING PLATE	
1- 6	2-626-294-01	+PTPWH 2.6*7	
1- 7	2-625-537-01	YOKE (S), SHUCKING	
1- 8	1-452-493-21	MAGNET	
1- 9	2-625-541-02	DAMPA	
1-10	2-625-548-02	CHUCKING PULLY	
1-11	X-2625-227-2	SUB CHASSIS ASSY (S)	
1-12	2-625-539-01	SPRING (S)	
1-13	2-625-730-01	SCREW	
1-14		*VACANT*	
1-15		*VACANT*	
1-16		*VACANT*	
1-17	2-625-552-07	AUTO SAD MAIN CHSSIS (S)	
1-18	3-319-501-51	SCREW + PTPWH 2.6X16	
1-19	2-625-547-03	DRIVER GEAR (S)	
1-20	2-625-545-04	CONTROL CAM (S)	
1-21	1-692-667-11	LEAF SW	
1-22	1-564-721-11	PIN, CONNECTOR 5P	
1-23	1-640-523-12	LOADING PWB (S)	
1-24	X-2625-117-1	MOTOR ASSY, LOADING	
1-26	2-625-536-02	LOADING PULLY	
1-28	2-625-279-01	SCREW +B2.6X2.5	

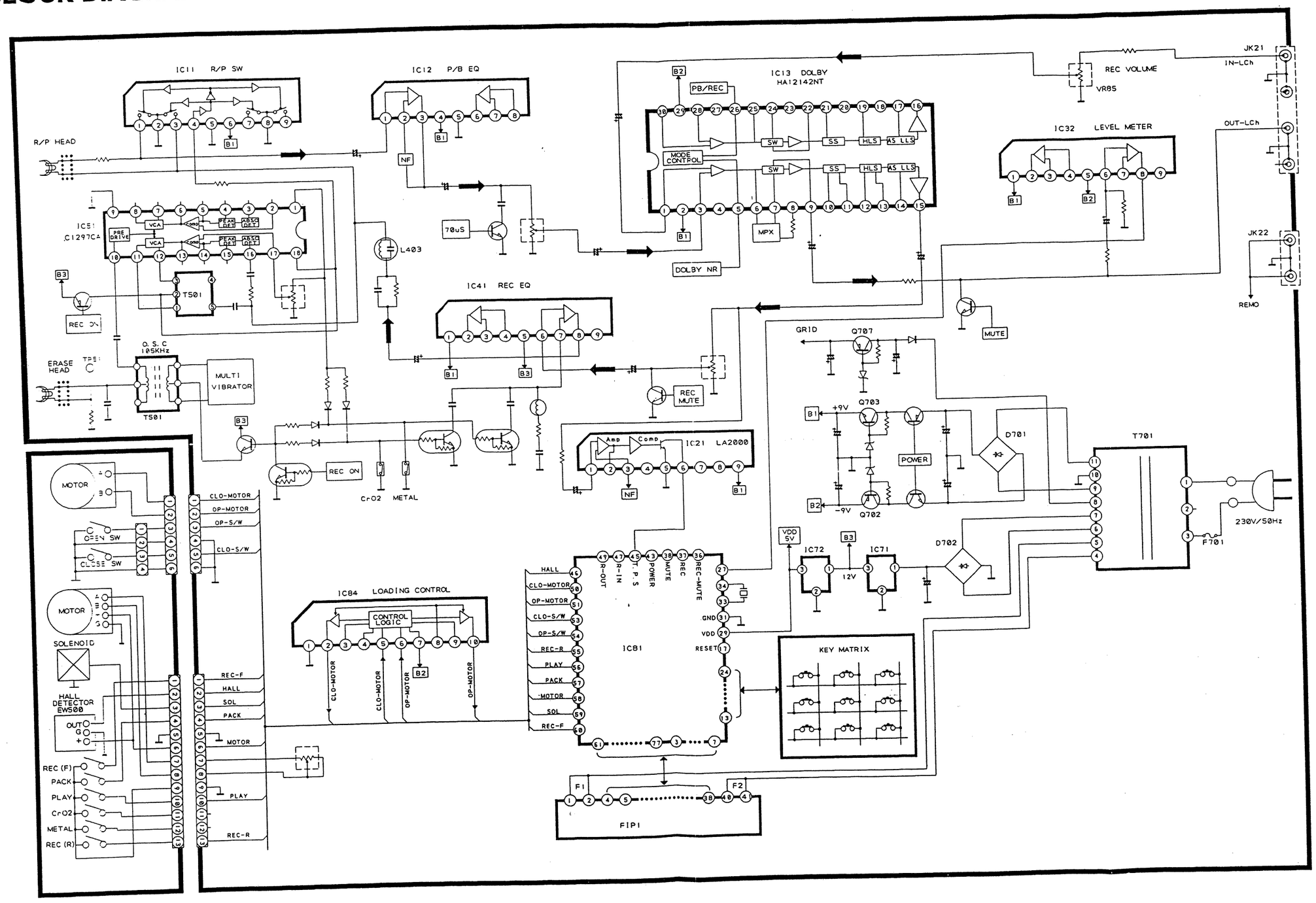
EXPLODED VIEW



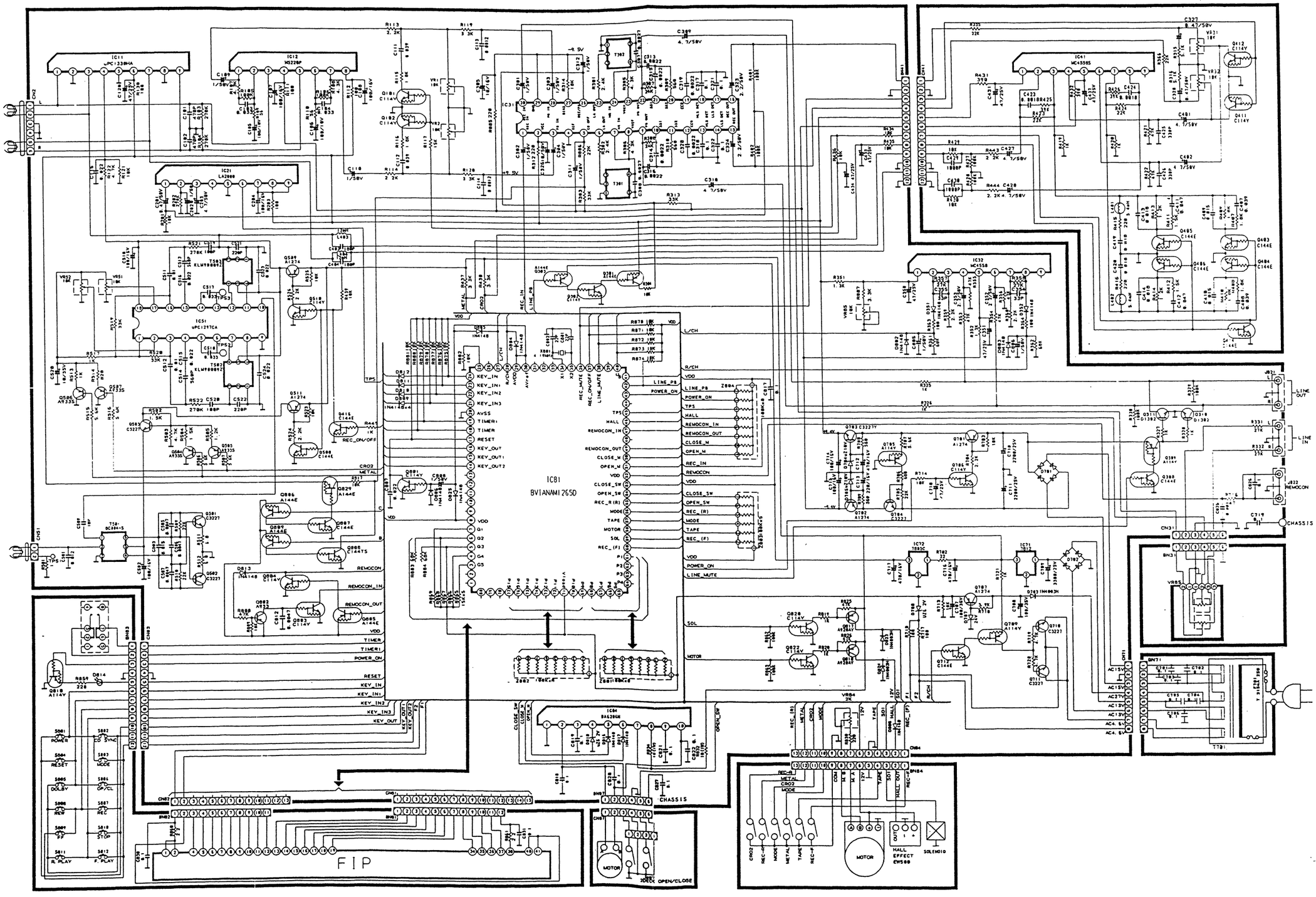
NO	PARTS - NO	DESCRIPSION	Q'Ty	MODEL NO.
1	KGX1A2727C19	ORNAMENT,DOOR	1	
2	KGR1A152K17	DOOR,CD	1	
3	KGU1A214A5Z	WINDOW,FIP	1	
4	KGR1A082	BADGE	2	
5	KKM2A0917C19	PANEL,AL	1	
6	KGV1A1262M7K78	PANEL,SUB	1	
7				
8	KGL1A120	INDICATOR,POWER	1	
9	KBT1A647M7K78	KNOB,POWER	1	
10	KBT1A648M7ZK78	KNOB,OPEN	1	
11	KBT1A649M7K78	KNOB,STOP	1	
12	KBT1A650M7ZK78	KNOB,PLAY	1	
13	KHD1A374	BRACKET,FLT	2	
14	KHH1A086	SUPPORT,MECHA	2	
15	KHE1A023	MOUNT,PCB	3	
16	KKL1A047M7H8	FOOT	4	
17	KHG1A039Z	FOOT,RUBBER	4	
18	KUA2A137	MAIN CHASSIS	1	
19	KKC3B077S29	CABINET,TOP	1	
20	KKF3A127P	PANEL,REAR	1	
21	KHR129	BUSHING,AC CORD	1	
22		CORD,POWER	1	
23	B,DKSL-210ABM	CD MECHANISM ASS'Y	1	
24	KHG1A163	RUBBER,SUPPORT	2	
25	KHG1A115	RUBBER	1	
26	KHG1A167	RUBBER,CUSHION	1	
27				
28				
29				
30				
31				
32				
33		SUB PCB ASS'Y	1	
34		MAIN PCB ASS'Y	1	

S1	KTB3+6J	SCREW	3	
S2	KTS3+8J	SCREW	4	
S3	KTB3+10G	SCREW	14	
S4	KTB3+8J	SCREW		
S5	KKD1A016	SCREW	4	
S6	KTB3+14J	SCREW	2	
S7	KTV3+8J	SCREW	7	
S8	KTB4+6FFZ	SCREW	4	
S9	KTB4+8F	SCREW	3	
S10	KTB3+6F	SCREW	4	
S11	KTB3+8JFZ	SCREW	3	
S12	KTB3+10GFZ	SCREW	5	

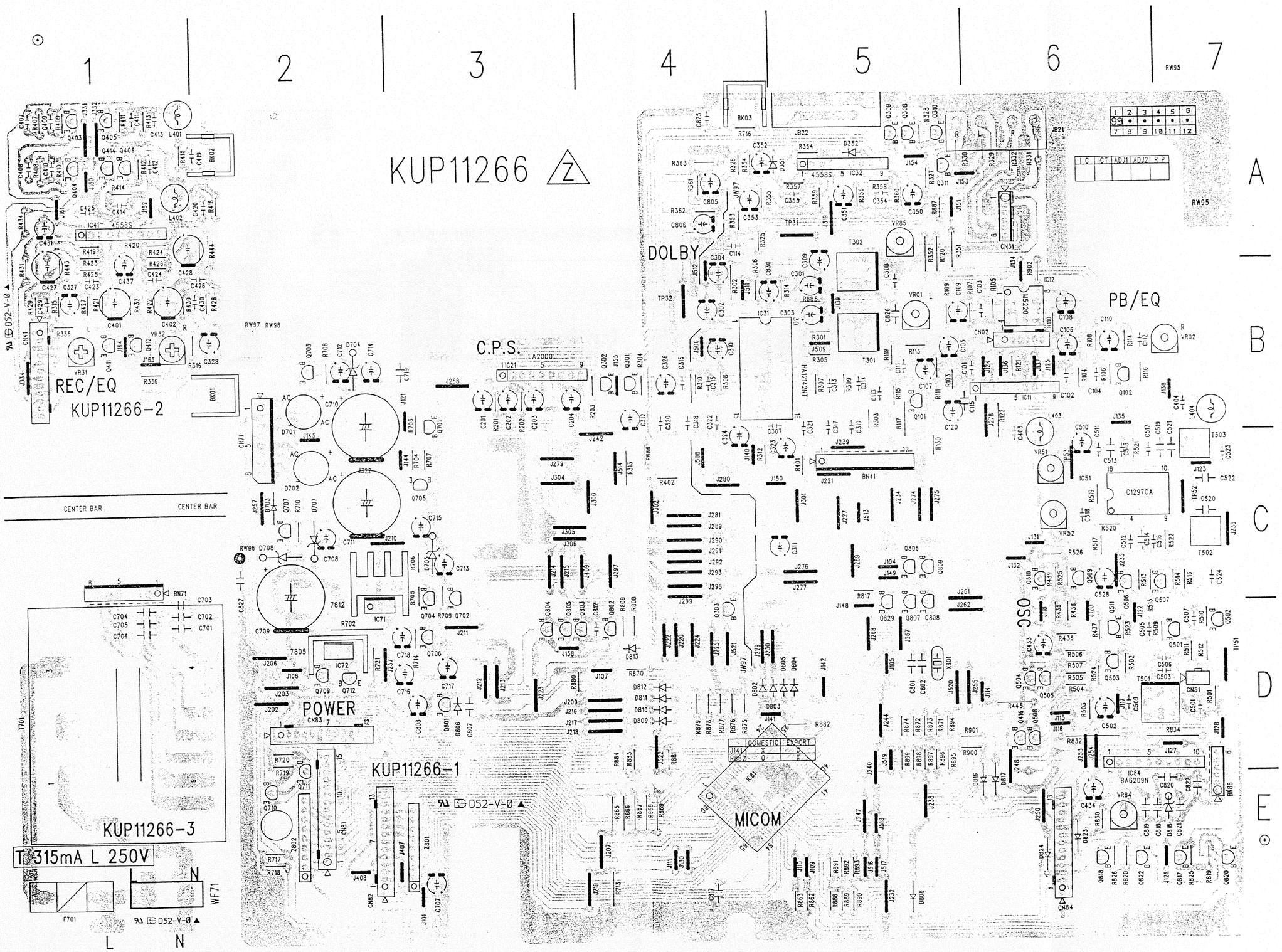
BLOCK DIAGRAM

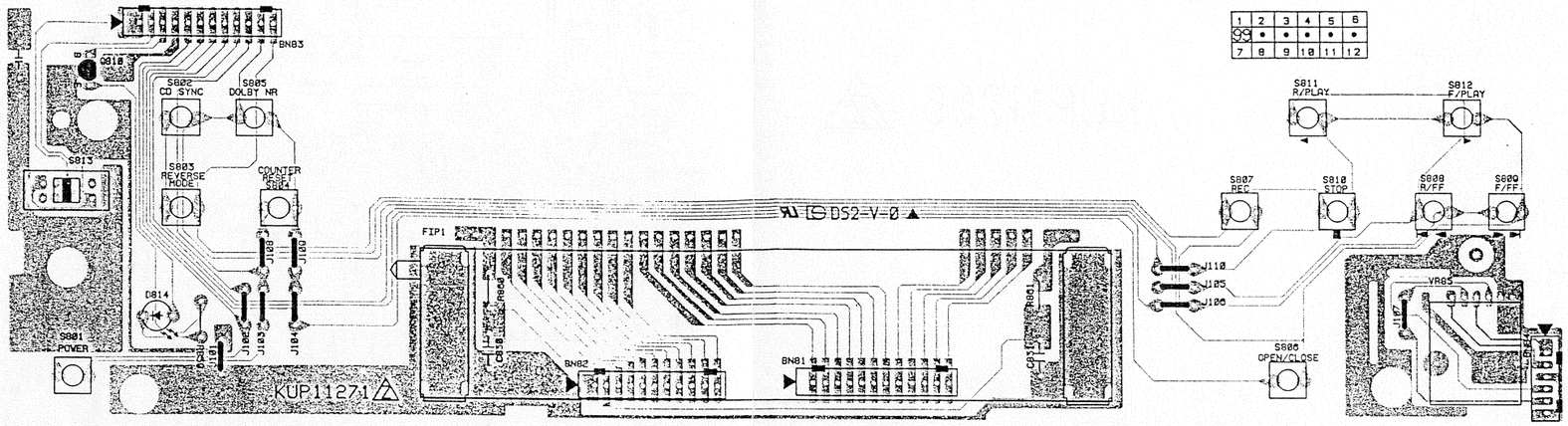


SCHEMATIC DIAGRAM

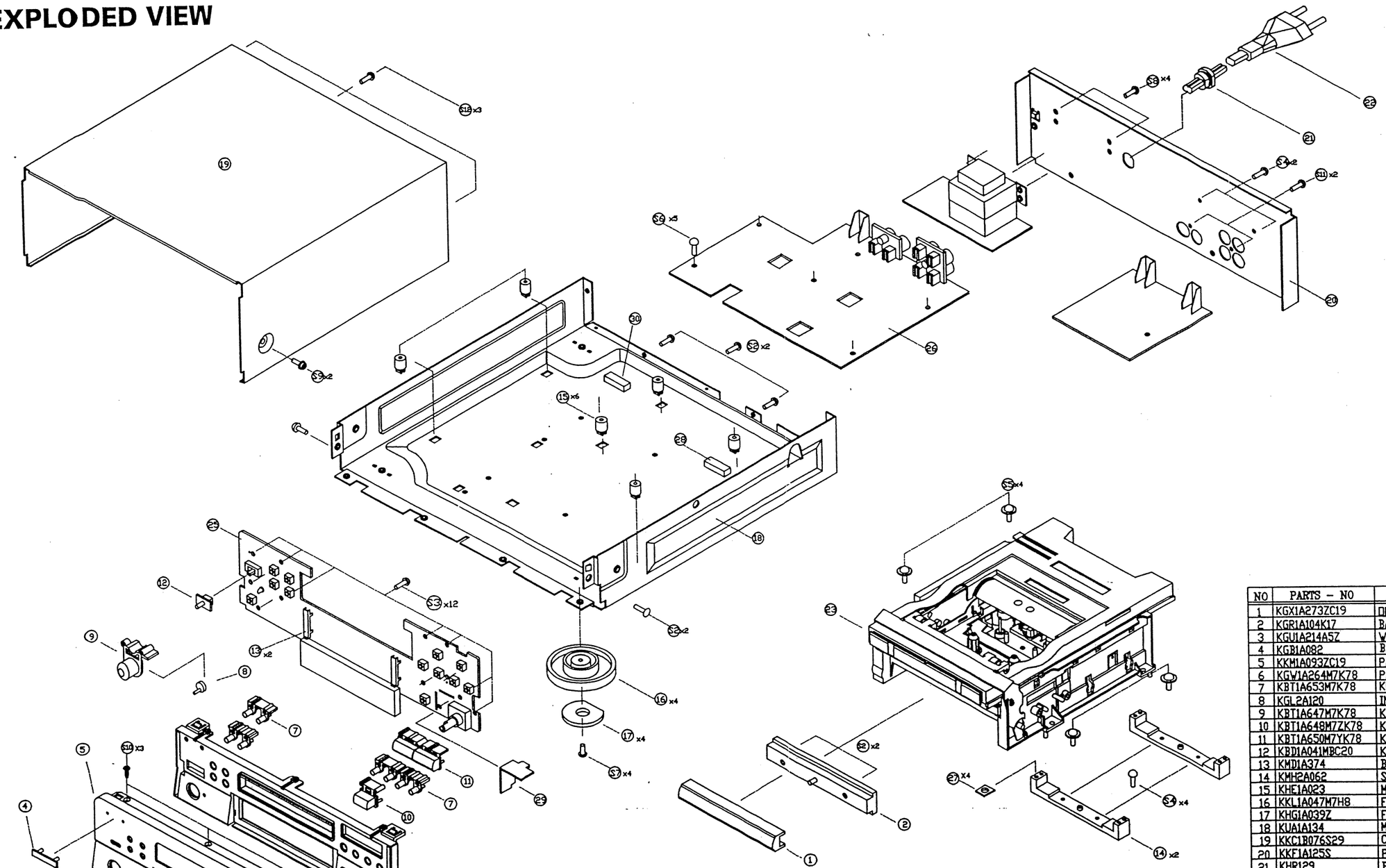


PRINTED DIRCUIR BOARDS




BN83
S818
S802
CD SYNC
S805
DOLBY NR
S813
S803
REVERSE
MODE
COUNTER
RESET
S804
D814
S801
POWER
KUP11271
FIP1
DS2-V-0
BN82
BN81
S811
R/PLAY
S812
F/PLAY
S807
REC
S810
STOP
S808
R/FF
S809
F/FF
S806
OPEN/CLOSE
VR85
1 2 3 4 5 6
7 8 9 10 11 12

EXPLODED VIEW



NO	PARTS - NO	DESCRIPSION	Q'Ty	REMARKS
1	KGX1A273ZC19	ORNAMENT, DOOR	1	
2	KGR1A104K17	BASE, DOOR	1	
3	KGU1A214A5Z	WINDOW	1	
4	KGB1A082	BADGE,UNIVERSUM	1	
5	KKM1A093ZC19	PANEL,FRONT	1	
6	KGW1A264M7K78	PANEL,SUB	1	
7	KBT1A653M7K78	KNOB,CPS	2	
8	KGL2A120	INDICATOR,POWER	1	
9	KBT1A647M7K78	KNOB,POWER	1	
10	KBT1A648M7ZK78	KNOB,OPEN	1	
11	KBT1A650M7YK78	KNOB,PLAY	1	
12	KBD1A041MBC20	KNOB,SLIDE	1	
13	KMD1A374	BRACKET,FLT	2	
14	KMH2A062	SUPPORT,MECHA	2	
15	KHE1A023	MOUNT,PCB	6	
16	KKL1A047M7H8	FOOT	4	
17	KHG1A039Z	FOOT,RUBBER	4	
18	KUA1A134	MAIN CHASSIS	1	
19	KKC1B076S29	CABINET,TOP	1	
20	KKF1A125S	PANEL,REAR	1	
21	KHR129	BUSHING,AC CORD	1	
22	KJA2B019Z	CORD,POWER	1	
23	KJDADH5000R/P	FL MECHA' ASS'Y	1	
24	KGX2A274ZA	ROTARY KNOB CAP ASS'Y	1	
25	KDP11271B	SUB PCB ASS'Y	1	
26	KDP11266B	MAIN PCB ASS'Y	1	
27	KHG1A115	MECHA, RUBBER	4	
28	KHG1A104	CUSHION,SUPPORT	1	
29	KMC1A155	PLATE, SHIELD	1	
30	KHG1A080Z	CUSHION	1	
31				
32				
33				
34				

S1	KTS3+8J	SCREW	4	
S2	KTB3+6J	SCREW	6	
S3	KTB3+10G	SCREW	12	
S4	KTB3+8JFZ	SCREW	6	
S5	KHD3A009	SCREW,SPECIAL	4	
S6	KTW3+16G	SCREW	5	
S7	KTW3+8J	SCREW	4	
S8	KTB4+8FFZ	SCREW	4	
S9	KHD1A024FC	SCREW,SPECIAL	2	
S10	KTS3+8G	SCREW	7	
S11	KTB3+10GFZ	SCREW	2	
S12	KTB3+8JFC	SCREW	3	
S13				
S14				